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Semiconductor Measurement Technology:

The Design, Testing, and Analysis of a Comprehensive Test Pattern for Measuring CMOS/SOS Process Performance and Control

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Semiconductor Measurement Technology:

The Design, Testing, and Analysis of a Comprehensive Test Pattern for Measuring CMOS/SOS Process Performance and Control

Loren W. Linholm

Electron Devices Division
Center for Electronics and Electrical Engineering
National Engineering Laboratory
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Semiconductor Measurement Technology: The Design, Testing, and Analysis of a Comprehensive Test Pattern for Measuring CMOS/SOS Process Performance and Control

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A Process Validation Wafer (PVW) is a wafer containing only test patterns. One PVW accompanies a product lot during the fabrication process. Test patterns NBS-16 and NBS-26 are designed to be used on PVWs. They contain both process parameter test structures and random fault test structures. Eighteen NBS-16 PVWs were fabricated in a radiation-hardened silicon-gate CMOS/SOS process. These PVWs were tested on a high-speed computer-controlled dc test system. Test results from the process parameter test structures were used to establish the baseline electrical parameters for each product lot and to produce an eight-level gray-scale wafer map for these parameters. Based on correlations of selected wafer maps, it was possible to identify specific yield-related process problems otherwise unknown to the manufacturer or user.

Test results from two random fault test structures were used to establish a statistically significant data base for identifying and evaluating major yield-limiting fault mechanisms in the process. Test results from a developmental random access fault structure and a gate dielectric integrity array are presented. The results are analyzed for selected PVWs and a major yield-limiting fault mechanism detected. A description of the test pattern and test results, including a drawing of each test structure, recommended test procedure, and design rules, are found in the appendices.

Key words: integrated circuits; microelectronics; process validation wafer; random faults; silicon-on-sapphire; test pattern; test structure; yield.

1. INTRODUCTION

With the increasing complexity of integrated circuits, it is becoming more difficult for both the manufacturer and user to fully characterize circuit performance. Functional testing alone is an impractical approach for evaluating complex circuits. As a result, greater emphasis is being placed on results from microelectronic test structures which provide clear and unambiguous test results [1].

The objective of the work covered in this report was to develop process assessment methods which use microelectronic test structures and which can be used by an independent organization to evaluate the electrical characteristics and yield potential of the integrated circuits being manufactured.

2. APPROACH

The approach used in meeting the objective of this program was to design, test, and evaluate a test pattern consisting of many well-defined and well-characterized test structures together with several developmental test structures. Test pattern NBS-16 was implemented as a process validation wafer (PVW) [2,3], a wafer consisting only of identical test patterns. One PVW was processed as part of each production run at RCA in a developmental program being conducted under Air Force Wright Aeronautical Laboratories (AFWAL) contract. The PVW was subsequently tested and evaluated at NBS. Midway through the program, a modified test pattern, NBS-26, was designed based on the information and experience gained from testing NBS-16.

The test pattern was designed in a collaborative effort by NBS and the Jet Propulsion Laboratory (JPL). Three areas on the test pattern contain structures designed by JPL. These structures were merged with four areas containing NBS-designed structures. Final pattern layout was performed by NBS. Testing and analysis of the structures was to be performed by the respective laboratories. Only the test results and analysis of the NBS structures are included in this report.

An automatic computer-controlled integrated circuit tester and wafer prober were used to determine the dc electrical parameters of selected test structures. Each test pattern on a wafer was probed and electrical results recorded on a line printer and floppy disc. Statistical analysis and wafer mapping of selected electrical parameters which formed a statistically significant data base were used to evaluate the process.

3. TEST PATTERN DESCRIPTION

3.1 Test Pattern NBS-16

NBS-16 is a square test pattern 250 mil (6.35 mm) on a side. It is divided into seven basic areas as shown in figure 1. Each area can be physically separated, if desired. The functions of each individual area are listed in table 1. A computer-generated plot of NBS-16 is shown in figure 2.

NBS-16 was fabricated in a radiation-hardened, silicon gate CMOS/SOS process. RCA uses a seven-level mask set for their radiation-hardened process. The process [4] has nine photolithography steps* (two masks are used twice). In the standard RCA process, the N-I mask is used for the n^- and p^+ implants and the P-I mask used for the p^- and n^+ implants. A list of the topological design rules and tolerances employed in designing the test pattern can be found in Appendix A. In this appendix as in this report, the terms polysilicon and poly are used interchangeably as are episilicon, epi, epi island, and island.

For optimum flexibility, the test pattern mask set contains nine levels as listed in table 2. This allows for n^+ into n^- and p^+ into p^- implants. It does not require any additional lithography processing and is fully

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*During the program, the n^- photolithography step and accompanying n^- implant were dropped, reducing the number of steps to eight.

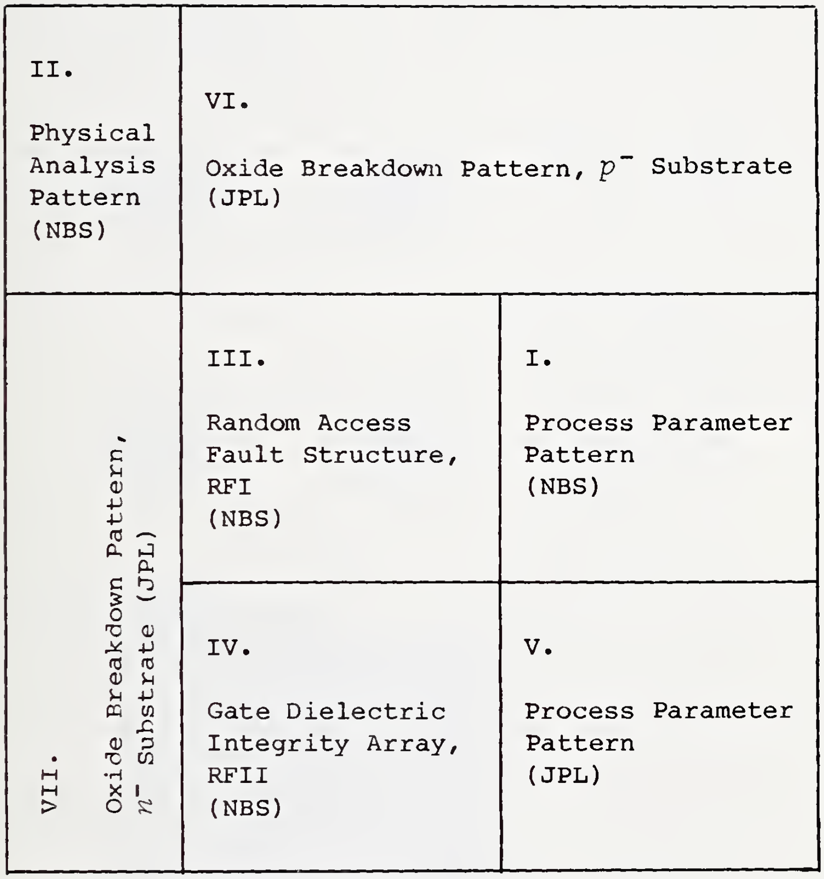
II.
Physical Analysis Pattern (NBS)
VI.
Oxide Breakdown Pattern, p^- Substrate (JPL)
VII.
Oxide Breakdown Pattern, n^- Substrate (JPL)
III.
Random Access Fault Structure, RFI (NBS)
I.
Process Parameter Pattern (NBS)
IV.
Gate Dielectric Integrity Array, RFII (NBS)
V.
Process Parameter Pattern (JPL)

Figure 1. Test pattern NBS-16 functional layout.

Table 1. Device Types on NBS-16.

	Area	Types of Devices
I.	Process Parameter Pattern (NBS)	MOSFETs, cross-bridge sheet resistors, contact resistors, capacitors, RCA Gate Universal Array Cells
II.	Physical Analysis Pattern (NBS)	Level designators, alignment marks, ion beam areas, surface profilometer, etch structure
III.	Random Access Fault Structure, RFI (NBS)	*p*- and *n*-channel MOSFETs
IV.	Gate Dielectric Integrity Array, RFII (NBS)	Capacitors
V.	Process Parameter Pattern (JPL)	MOSFETs, capacitors, resistors
VI.	Oxide Breakdown Pattern (JPL)	Capacitor array, p^- substrate
VII.	Oxide Breakdown Pattern (JPL)	Capacitor array, n^- substrate

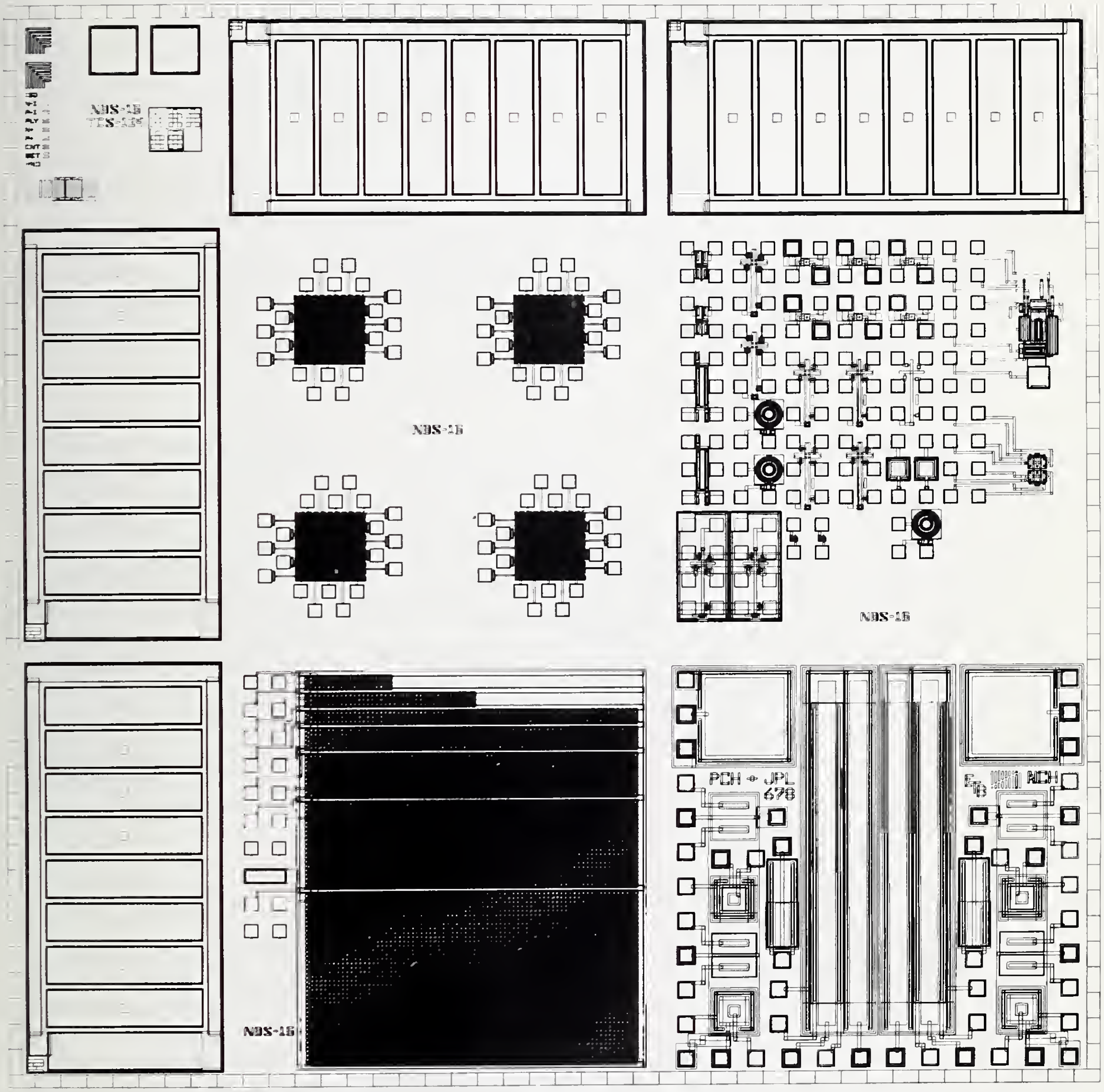

Figure 2. Computer-generated plot of test pattern NBS-16.

Table 2. Photomask Levels.

Process Step	Function	Mask Designator
1.	Island Definition	ISD
2.	n^- Implant	N-I
3.	p^- Implant	P-I
4.	Poly Definition	PLY
5.	n^+ Implant	N^+
6.	p^+ Implant	P^+
7.	Contact	CNT
8.	Metal Definition	MET
9.	Passivation	PRO

compatible with most commercial CMOS/SOS processes. The working photomasks were fabricated by a computer-controlled optical pattern generator at RCA.

The PVW was fabricated on 3-in. (76.2-mm) diameter silicon-on-sapphire wafers. Ninety-five of the 97 sites available on the PVW are used for NBS-16 test patterns. A detailed description of the test structures included on NBS-16, as well as the function, location, test method, and layout, is provided in Appendix B. A pattern designed by the manufacturer is located in the two remaining sites. This pattern includes a ring oscillator circuit and MOSFETs with varying gate lengths.

One PVW accompanied each product lot during fabrication. Upon completion, the wafer was tested in order to determine the value of critical electrical process parameters. These parameters were then statistically analyzed to identify correlations between selected parameters and the performance of the process lot. A total of 18 NBS-16 PVWs have been manufactured from 17 different process lots. In one instance, two PVW wafers accompanied the same product lot.

3.2 Test Pattern NBS-26

NBS-26 is identical to test pattern NBS-16 except for modifications to the process parameter pattern. A computer-generated plot of NBS-26 is shown in figure 3. Two test structures (no. 27, internal cell from RCA Gate Universal Array (GUA), and no. 28, input/output cell with input protection from RCA GUA) found on NBS-16 were omitted. In their location test structures consisting of p- and n-channel MOSFETs with 0.20-mil (5.08-μm) and 0.15-mil (3.81-μm) gate lengths, metal step coverage structures, and developmental MOSFET/cross-bridge sheet resistor test structures were added. These structures are also described in Appendix B. Eleven wafers containing NBS-26 test patterns were fabricated and tested. All 11 wafers were fabricated in the same lot and were used as a check of the functionality of the photomask set. At the time of this report, no NBS-26 test patterns had been fabricated as PVWs accompanying product wafer lots.

4. ELECTRICAL MEASUREMENTS AND ANALYSIS TECHNIQUES

4.1 Measurement System Description

The measurement system used to test the PVWs consists of a minicomputer and associated electrical test equipment. A block diagram of the measurement system is shown in figure 4. The minicomputer is configured with 352 kilobytes of memory, two 10-megabyte disc drives, two floppy disc drives, a 9-track dual density magnetic tape drive, a system console, several CRT and hard-copy terminals, a line printer, a digital plotter, and a multiuser operating system. The test equipment consists of an automatic wafer prober which can be programmed in English or metric units; a current supply with 1-μA resolution and compliance voltage programmable up to 100 V; two voltage supplies with 1-mV resolution and 550-mA current capability; a digital voltmeter with 1-μV resolution and operating modes which provide either high precision or high speed readings; a digital picoammeter with 1-pA resolution; 16 single-pole, single-throw dry reed relays; and eight 20-channel scanners, all digitally programmable and operating under computer control.

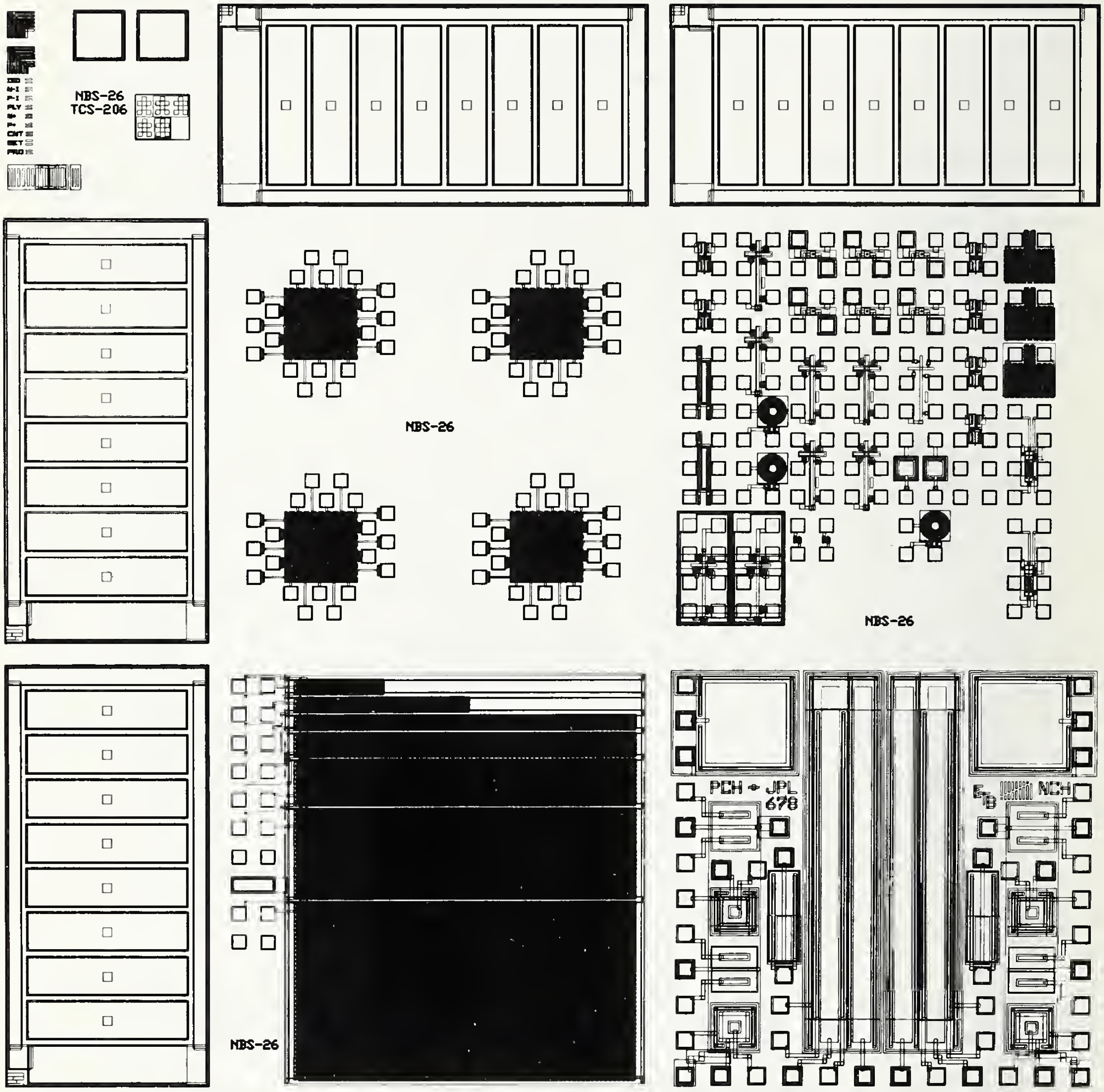

Figure 3. Computer-generated plot of test pattern NBS-26.

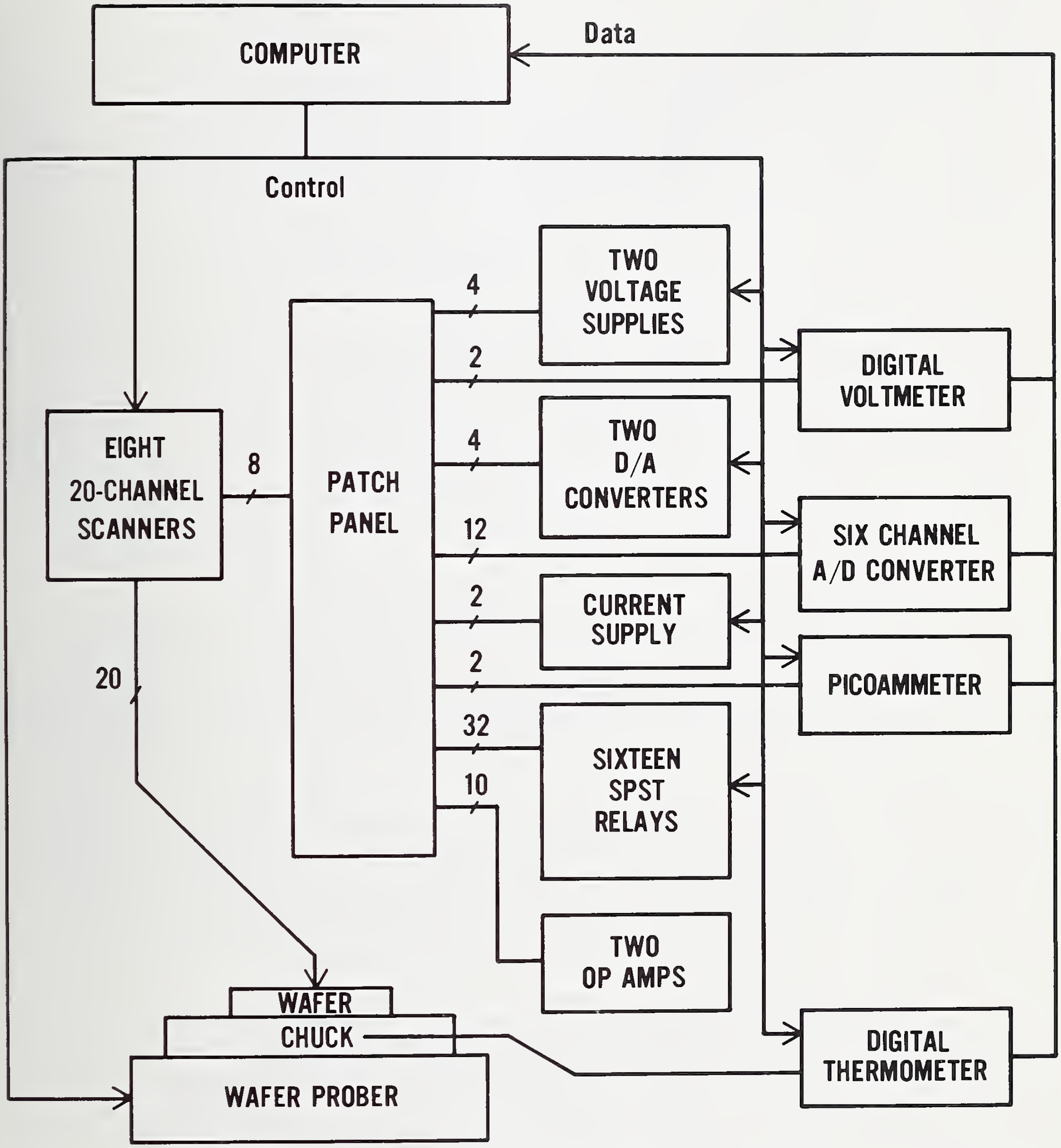

Figure 4. Block diagram of computer-controlled electrical test system.

The software to control these instruments consists of a set of assembly language subprograms, one to control each instrument; several assembly language subroutines for mathematical operations such as conversion from binary coded decimal to floating point format, status checking, and error handling; and a driver within the operating system. To activate an instrument, the user calls the appropriate subprogram from a FORTRAN program using a CALL statement. The instruments can also be controlled from programs written in BASIC. An interactive mode is available wherein the operator can command all instruments from a terminal. This is useful in developing and debugging software and in determining appropriate applied voltage or current levels for automated testing.

In a typical measurement, data are acquired from selected structures at each test site on a wafer, and the test results are logged to the line printer and recorded on a floppy disc. Testing time is determined by the data acquisition rate and the total number of sites tested. The data acquisition rate is generally limited by the response time of the test instrument which is usually run in a high precision or filtered mode. Typical measurement times for the digital voltmeter operating in the filtered mode are about one-half second per measurement; for the digital picoammeter, about eight seconds. When measurement precision and accuracy are not critical, the measurement time can be greatly reduced by operating instruments in an unfiltered mode.

4.2 Statistical Analysis Techniques

Once data are obtained, it is important to transfer this information into a form which can be readily interpreted by the user or manufacturer. Data analysis programs were developed to allow for the rapid determination of statistically significant parameters and to characterize their spatial variation over the wafer for further process analysis.

The program developed, called STAT2, allows one to determine the maximum, minimum, mean, and median values, the sample standard deviation (σ), and the percent standard deviation of each parameter. A 50-character histograph can be produced to permit the user to see how the data are distributed between the minimum and maximum values. A value N can be selected such that all points farther than N times the sample standard deviation from the mean can be identified.

For this work, all parameters measured except for leakage current were assumed to have a Gaussian distribution. In order to separate and identify devices which had failed and remove them from the data set from which meaningful statistical analysis could be performed, it was necessary to specify an exclusion criterion. For this work a device parameter was considered not to be representative of the baseline process if the parameter was outside a $\pm 3\sigma$ limit about the mean value for that parameter. On the average, for a population of 95 independent samples, the expected number of points that would fall outside this limit is between 0 and 1. This limit was considered a reasonable basis for identifying and separating data from the original population. When such data were present, the data were excluded from the population and the mean recomputed. This process was repeated until no points outside a $\pm 3\sigma$ bound were found.

This data base was then used to produce an eight-level gray-scale wafer map as shown in figure 5. For this figure, each "×" represents the location of a measured structure. Averaging techniques were used to determine the shading for sites excluded from the data population or locations not measured. The magnitude of each of eight levels is determined initially by simple division of the parameter range between maximum and minimum values. In order to produce wafer maps which represent parameter variations over a predetermined range of interest, the upper bound of the highest level and the lower bound of the lowest level can be varied by the operator. When the bounds are varied, a "+" is used to denote the location of a structure with a parameter magnitude greater than the highest level of the upper bound, and a "-" is used to denote the location of a structure with a parameter magnitude below the lower bound of the lowest level.

5. EVALUATION

5.1 Process Parameter Pattern

In order to control a developmental integrated circuit process, a process engineer must:

(a) identify which parameters accurately predict or determine the degree of process control;
(b) establish the value and range, etc., of these parameters for a given process lot; and
(c) determine how these values vary across an integrated circuit die, across a wafer, from wafer to wafer, and from lot to lot.

Test results must be obtained and interpreted in a timely fashion in order to be used for correcting or improving the process. A PVW containing appropriate process parameter test structures can be used to obtain test results which provide:

(a) a statistically significant estimate of the value and range of critical process parameters;
(b) the variation in these parameters as a function of wafer location; and
(c) the lot-to-lot variation in critical parameters.

As will be shown later, the spatial variation of critical parameters can be used to establish correlations between different parameters and allow identification and evaluation of wafer processing problems. In some instances the spatial variation of certain parameters can be used to infer the variability of parameters which cannot otherwise be determined by test structures or test methods that are available.

For this work, the process parameter patterns on 18 NBS-16 PVWs (wafers A1 through A18) from 17 different lots were evaluated. Wafers A16 and A18 were processed in the same product lot. The process parameter patterns from one entire lot of 11 NBS-26 test patterns (wafers B1 through B11) were also evaluated.

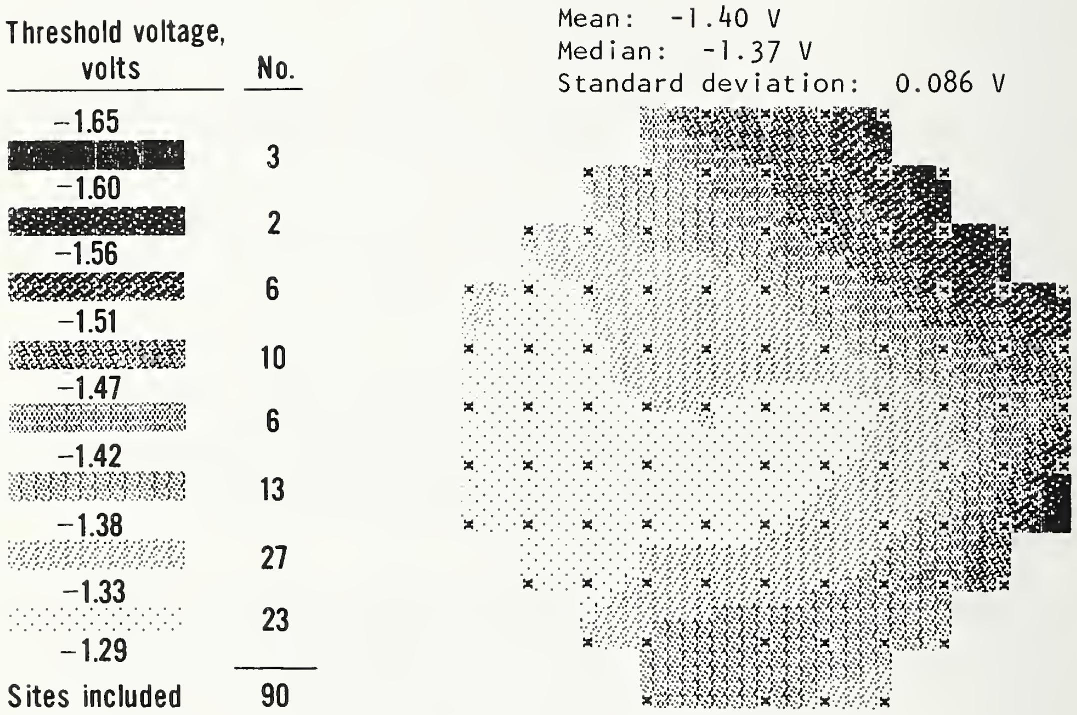

Figure 5. Typical computer-generated (eight-level) gray-scale wafer map showing test site location and intrawafer parameter variation.

The process parameter pattern included on NBS-16 in Area I is a square approximately 100 mil (2.54 mm) on a side and contains 28 test structures laid out in 2 by N probe-pad arrays [5]. The 2 by N probe pad array allows for the use of one common probe card for wafer probing. It also allows great ease and flexibility in test pattern design. For the process parameter pattern on NBS-16, N varies between 10 and 14 depending on the column. Testing was performed using a 2 by 10 probe card. The pattern on NBS-26 is of similar size and probe-pad arrangement and contains 35 test structures. The process parameter pattern for NBS-16 is shown in Appendix B, figure B-3, and for NBS-26 in Appendix B, figure B-4. A description of each test structure and corresponding test method employed in this study can also be found in this Appendix.

The test structures that were selected for inclusion in the process parameter pattern were those that were judged to provide the maximum number of useful process parameters within the available space on the test die and to minimize the testing constraints imposed by the automatic testing system. The test structures listed in table 3 were those which were evaluated to determine the baseline electrical characteristics of the process. Additional developmental structures were also included on the patterns. Test results from the process parameter pattern were obtained using the automatic wafer prober and data analysis techniques previously described. The parameters measured, described in Appendix B, were selected to provide information of sufficient accuracy while minimizing the testing time and test equipment utilization.

5.1.1 Lot-to-Lot Contact Resistance Variation

The lot-to-lot variation in critical parameters can be used to monitor the degree of process control. Plots of the lot-to-lot variation in the average metal-to-n^+ contact resistance (Device no. 19) and the average metal-to-p^+ contact resistance (Device no. 18) are shown in figure 6. Data presented are from PVWs A1 through A18. Each point plotted represents the average resistance of approximately 95 test structure measurements on each PVW. Since the contact resistor test structure [6] is a four-terminal Kelvin-type structure with current taps separated from voltage taps, the effects of probe-to-probe-pad contact resistance or the series resistance of the epi layer or metal layers connecting the probe pads to the voltage taps do not affect the measurement.

The test results indicate a wide range in the metal-to-n^+ contact resistance from lot to lot. Since little variation is observed in metal-to-p^+ contact resistance and because both contact resistors are adjacent devices, and the contact window is defined in the same photolithographic process for both structures, variations or problems with contact window photolithography, etching, and subsequent thermal processing are not suspected. The magnitude of the variations in metal-to-n^+ contact resistance indicates problems associated with other aspects of process control.

5.1.2 Intrawafer Contact Resistance Variation

Further information relating to the lot-to-lot contact resistance variation can be obtained by looking at the intrawafer variation in these parameters and establishing correlations with other process parameters. Wafer maps of

Table 3. List of Structures Evaluated on Process Parameter Patterns.

Structure No.	Description
1.	*p*-channel four five-terminal MOSFET
2.	*n*-channel four five-terminal MOSFET
3.	*n*-channel five-terminal MOSFET
4.	*p*-channel five-terminal MOSFET
9.	p^+ cross-bridge sheet resistor
10.	n^+ cross-bridge sheet resistor
11.	p^+ doped poly cross-bridge sheet resistor
12.	n^+ doped poly cross-bridge sheet resistor
13.	Metal cross-bridge sheet resistor
18.	Metal to p^+ contact resistor
19.	Metal to n^+ contact resistor
20.	Metal to p^+ doped poly contact resistor
21.	Metal to n^+ doped poly contact resistor
22.	*p*-type MOS capacitor
23.	*n*-type MOS capacitor

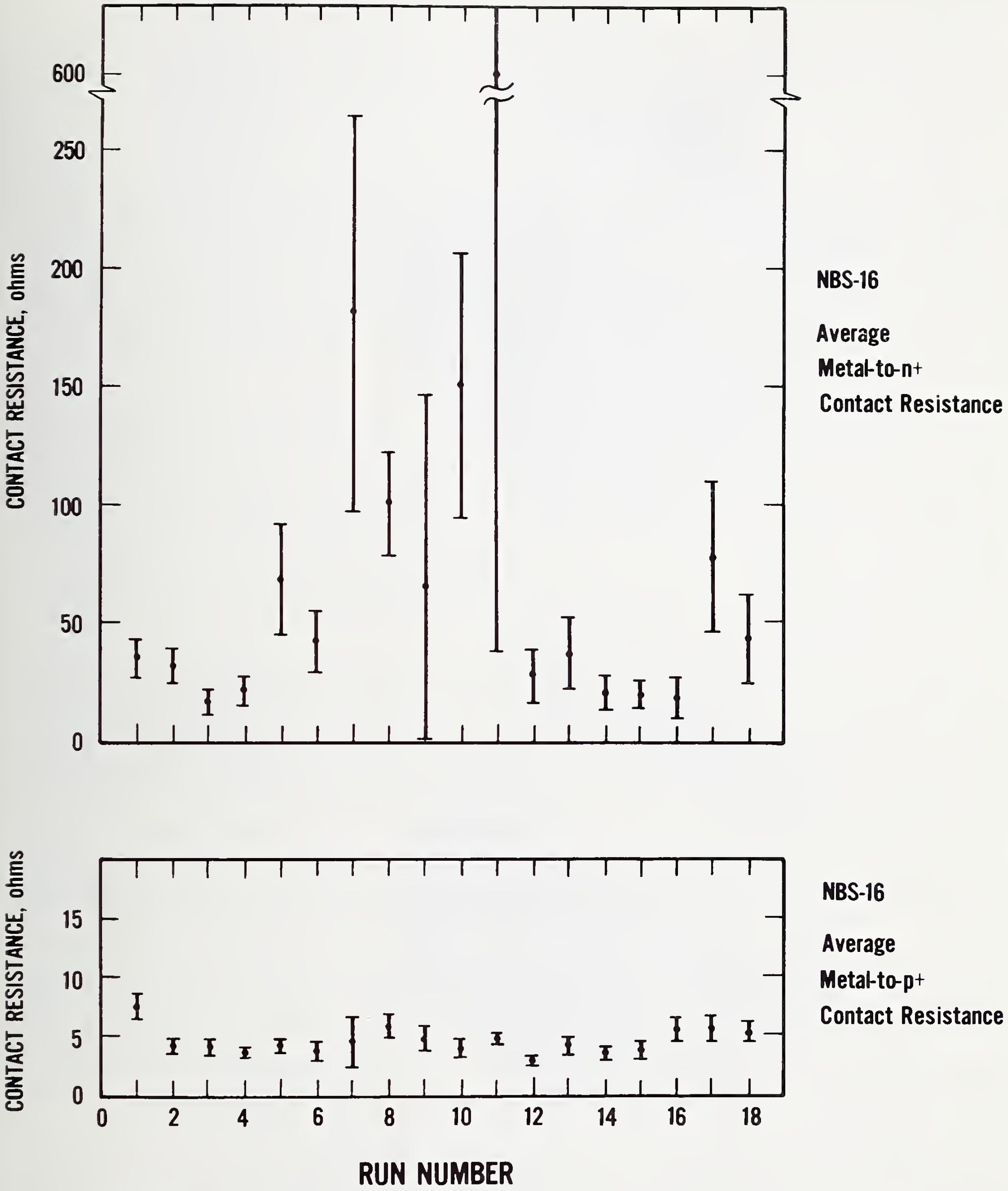

Figure 6. Average metal-to-n^+ contact resistance, Ω, *versus* lot number and average metal-to-p^+ contact resistance, Ω, *versus* lot number. Data presented show the variation in the electrical parameters over a time interval of approximately two years.

metal-to-n^+ contact resistance and n^+ sheet resistance for the PVWs accompanying lots A10 and A9 are shown in figures 7 and 8, respectively. For lot A10, both the mean and median values of metal-to-n^+ contact resistance and of n^+ sheet resistance are approximately equal. The approximate correlation of the map pair in figure 7 suggests that the high metal-to-n^+ contact resistance is a function of sheet resistance or phosphorus concentration.

For lot A9, as shown in figure 8, there is a large difference between the mean and median values for metal-to-n^+ contact resistance. Approximately two-thirds of the metal-to-n^+ contact resistance structures measured had a resistance below 40.7 Ω. The remaining structures with a resistance higher than this value are grouped in the lower right portion of the PVW. The shading scale used both in this illustration and in figure 7 was determined by dividing the range between the lowest and highest parameters obtained into eight segments of equal magnitude.

The accompanying n^+ sheet resistance data have approximately equal mean and median values suggesting a more symmetrical distribution of measured parameters. Here, the wafer map was produced by adjusting the minimum bound of the parameter shading range so that approximately the same number of points would be included for the first seven levels as for the first seven levels of the metal-to-n^+ contact resistance map. Values of n^+ sheet resistance falling below this bound are represented by the lightest gray tone. As can be seen in figure 8, the highest metal-to-n^+ contact resistance occurs in the regions of highest n^+ sheet resistance.

The sheet resistance of the measured structures was controlled by a two-stage phosphorus implant. The first implant was intended to dope the majority of the epi island region. The second was intended to increase the dopant concentration at the island surface in order to decrease contact resistance in source and drain regions. Both implants were made through a gate oxide which covered the epi island.

Subsequent capacitance measurements on the p-type MOS capacitor (Device no. 21) on the PVW from lot A9 indicated that the gate oxide thickness was greatest in the areas of lowest phosphorus concentration.

Based on this wafer map correlation, it was concluded that due to variations in the gate oxide thickness which were unaccounted for in the process design, the peak of the phosphorus implant varied between the silicon and silicon dioxide depending upon the oxide thickness. This caused significant variations in the amount of phosphorus reaching the silicon surface during the implant and caused the observed variation in metal-to-n^+ contact resistance.

5.1.3 Lot-to-Lot p-Channel Threshold Voltage Variation

Wafer maps for one-parameter, p-channel threshold voltage of Device no. 1, for all 18 PVWs produced, are reproduced in Appendix C. These results are illustrative of how a single parameter can vary across a wafer and from lot to lot. The data presented are the p-channel threshold voltage of Device no. 1.

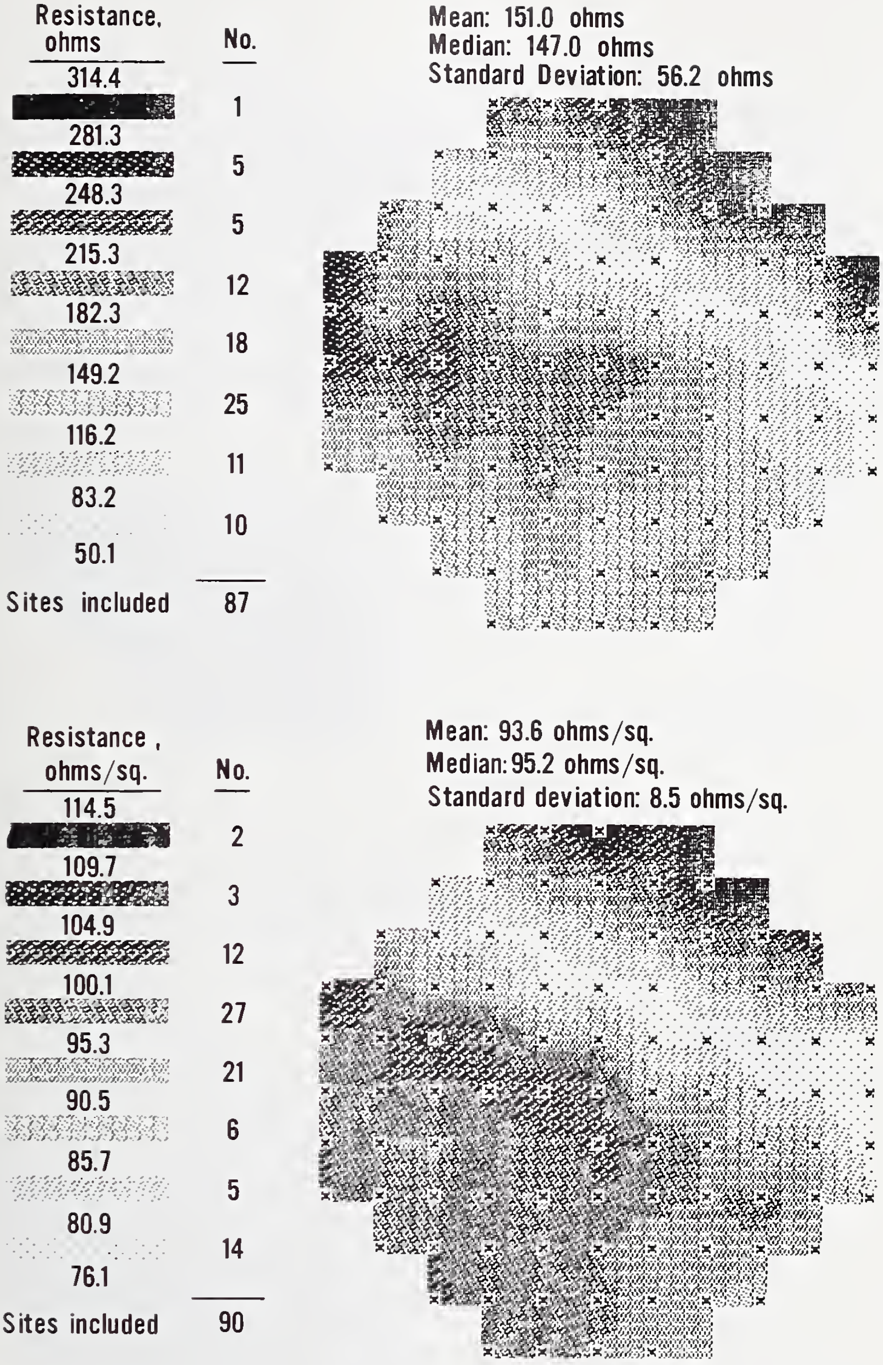

Figure 7. Wafer maps of metal-to-n^+ contact resistance (top) at 87 test sites and n^+ sheet resistance (bottom) at 90 test sites for NBS-16 PVW A10. In both maps, the scale or gray-tone boundaries were selected such that the upper bound of the darkest gray tone was the largest resistance value, and the lower bound of the lightest gray tone was the smallest resistance value. The "×" symbols on the maps represent the locations of nondefective test sites. Test results from these sites were used to calculate mean, median, and standard deviation and also to produce the wafer map.

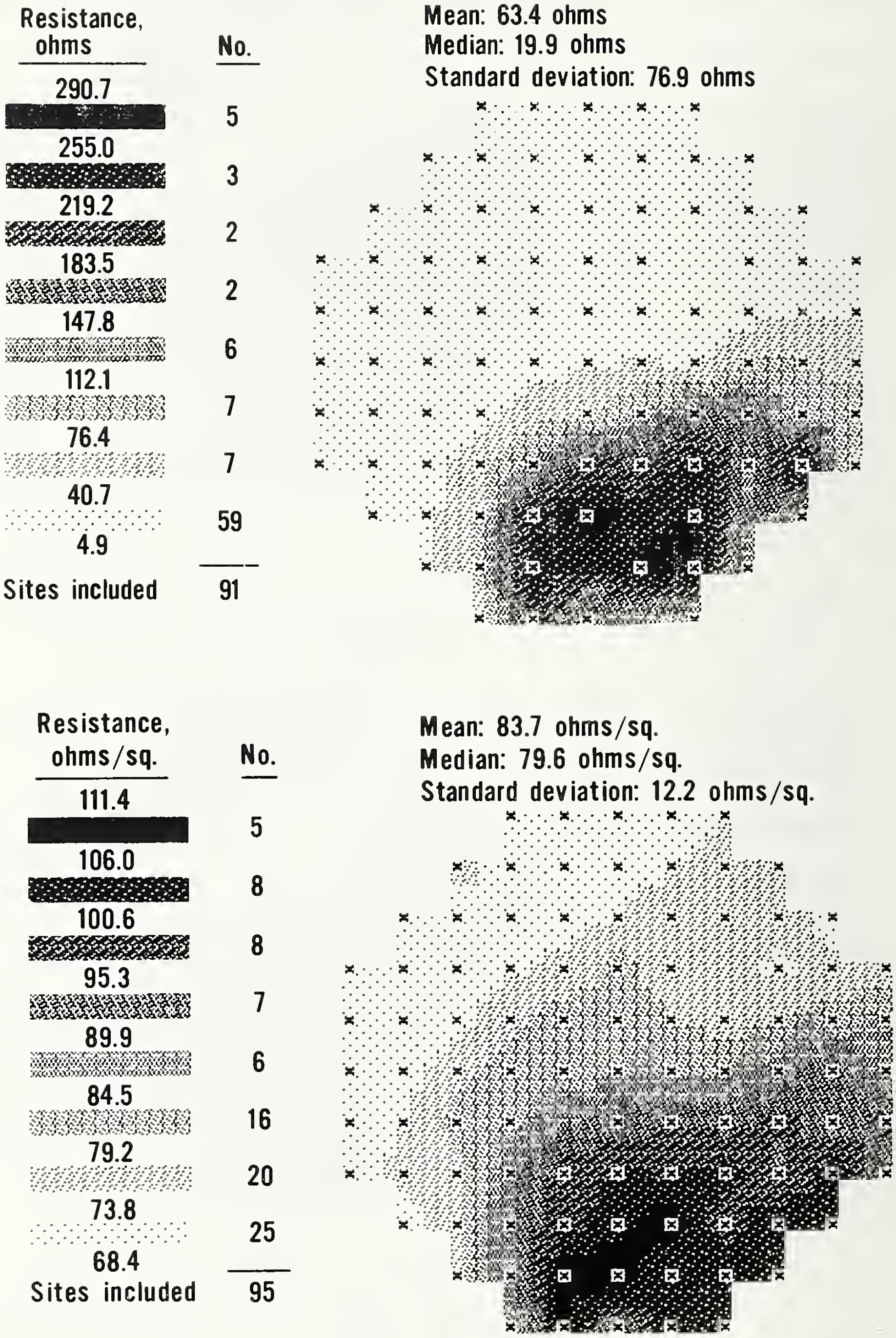

Figure 8. Wafer maps of metal-to-n^+ contact resistance (top) at 91 test sites and n^+ sheet resistance (bottom) at 95 test sites for NBS-16 PVW A9.

Two of these wafer maps of *p*-channel threshold voltage are shown in figure 9. As can be seen, a general similarity in the two maps exists with higher valued parameters located in the upper right of the map and lower valued parameters located in the lower left. A majority of the 18 wafer maps in Appendix C contain this general pattern. This suggests that usually the *p*-channel threshold voltage is affected by processes in which the wafers are all similarly oriented with respect to the wafer flat.

There are two areas in the fabrication in which wafers are processed with the wafer flat location remaining the same: photolithography and epitaxial growth. In general, threshold voltage variation correlating with a lithography variation is not expected for MOSFETs of the size (0.3 mil, 8 μm) being tested. Variations in linewidth of poly, epi, and metal can be found in the appropriate wafer maps in Appendix D which contains a complete set of wafer maps and statistical data. No correlation with threshold voltage was observed.

A simple expression for the threshold voltage of a *p*-channel silicon gate MOSFET is [7,8]:*

$$V_T = \phi_{ss} + \phi_B - \frac{Q_{ox}}{C_{ox}} - \frac{Q_B}{C_{ox}} \quad . \tag{1}$$

where ϕ_{ss} = effective work function of the silicon-oxide-silicon system,
ϕ_B = total band bending at the onset of strong inversion,
Q_{ox} = total surface state charge located at the silicon-silicon dioxide interface,
Q_B = charge contribution of the substrate depletion region, and
C_{ox} = the gate oxide capacitance.

In general, ϕ_{ss} is a function of the gate electrode material, polysilicon. The sum of both ϕ_{ss} and ϕ_B is approximately constant for a given gate electrode technology. C_{ox} for the most part varies with changes in the gate oxide thickness.

The main factors affecting the variation in Q_{ox} are substrate crystal orientation, oxidation conditions, and subsequent thermal processing. Q_B is given by

$$Q_B = (2\varepsilon_s \, q \, N_D \, [-\phi_B])^{1/2} \quad , \tag{2}$$

where ε_s = the permittivity of silicon,
N_D = the substrate dopant concentration, and
q = the electronic charge.

Thus, Q_B varies mainly with changes in the substrate dopant concentration.

Dopant concentration for the n^- islands is determined in the epitaxial growth process. No other epi island doping is intentionally performed. For this process, the wafer flat location relative to the gas injector within the

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* The cited references provide a more detailed description of the parameters affecting the threshold voltage.

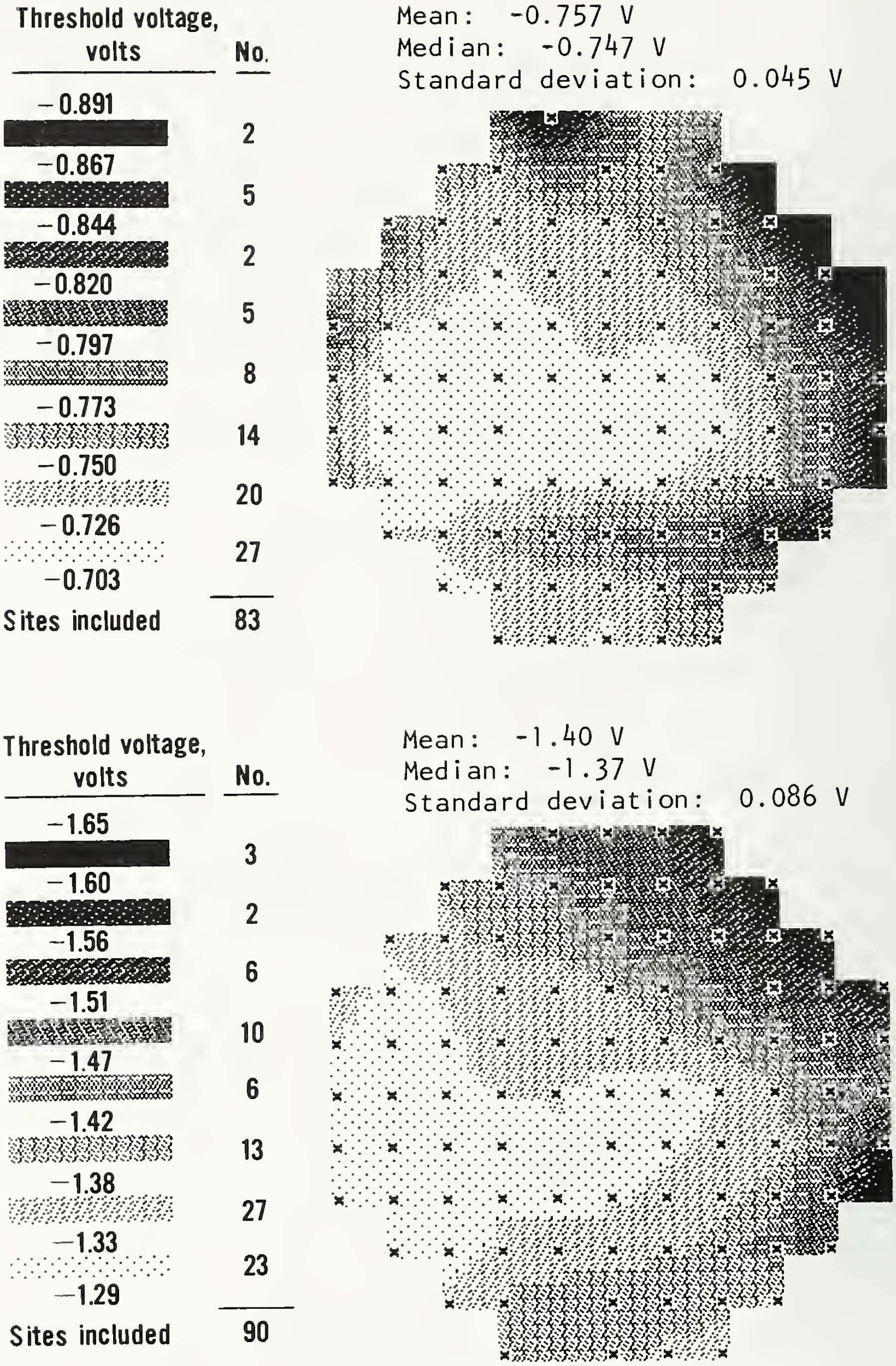


Figure 9. Wafer maps of *p*-channel threshold voltage at 83 test sites for PVW A16 (top) and PVW A11 (bottom).

epitaxial reactor is both the same for each wafer and the same from lot to lot. A pancake type of vertical reactor was used with a rotating susceptor. During the epitaxial growth process, if depletion of the dopant species were to occur across the susceptor, a systematic variation in the epi island dopant concentration across each wafer would occur.

Other factors which influence threshold voltage, such as Q_{OX} and C_{OX}, are governed by gate oxide growth, anneal, sinter, and poly deposition, processes which are performed with uncontrolled wafer flat orientation. If these processes were the major factors governing the variation in *p*-channel threshold voltage, similar variations in the *n*-channel threshold voltage would also be observed. Lot-to-lot variation in *p*-channel threshold voltage as a function of variation in Q_{OX} or C_{OX} is not anticipated because of the uncontrolled wafer orientation during the processes which affect these parameters. This observation is further supported by the lack of any correlation between *p*-channel and *n*-channel wafer maps for the same PVW. These test results suggest that the dominant source of variation in *p*-channel threshold voltage is the variation in epi island dopant concentration. The observed variation is consistent with the expected dopant variation introduced during epitaxial growth.

There are no test structures or test methods available from which the *n*-island concentration can be directly determined. By determining the variation of threshold voltage across the wafer and from wafer to wafer, it was possible to identify processing techniques which affected the control and variability of this critical quantity.

5.1.4 Intralot Parameter Variation

One 11-wafer lot of NBS-26 test patterns was produced in order to qualify the functionality of the mask set for NBS-26. Test results from the process parameter pattern indicated the presence of functional MOSFETs on three of the 11 wafers produced. Analysis of electrical tests on the remaining wafers indicated the absence of electrical contact between the device being tested and the wafer prober. Further analysis indicated that the metal cross-bridge sheet resistors (Device no. 13) on all 11 wafers were functioning properly and providing expected test results. These results indicate that adequate probe-to-probe-pad contact is being made and that the electrical problems being encountered are associated with the contact windows between metal and all other conductive layers. From visual inspection, it was determined that the contact window lithography step had been performed. The presence of a contact window problem was confirmed by test results from one of the PVWs containing functional devices.

Figure 10 contains wafer maps of *n*-channel threshold voltage and n^+ sheet resistance for PVW B4. The threshold voltage wafer map indicates that nonfunctional MOSFETs are clustered in the upper right portion of the map. Voltages exceeding 12 V for this measurement indicate that the voltage limit for the programmable current supply was reached due to an open circuit in the structure under test. Similarly, the n^+ sheet resistance shows the location of nonfunctioning cross-bridge resistors. Test results from the cross-bridge sheet resistors in the upper right portion of the PVW show that a voltage limit had again been reached. (For the van der Pauw sheet resistance

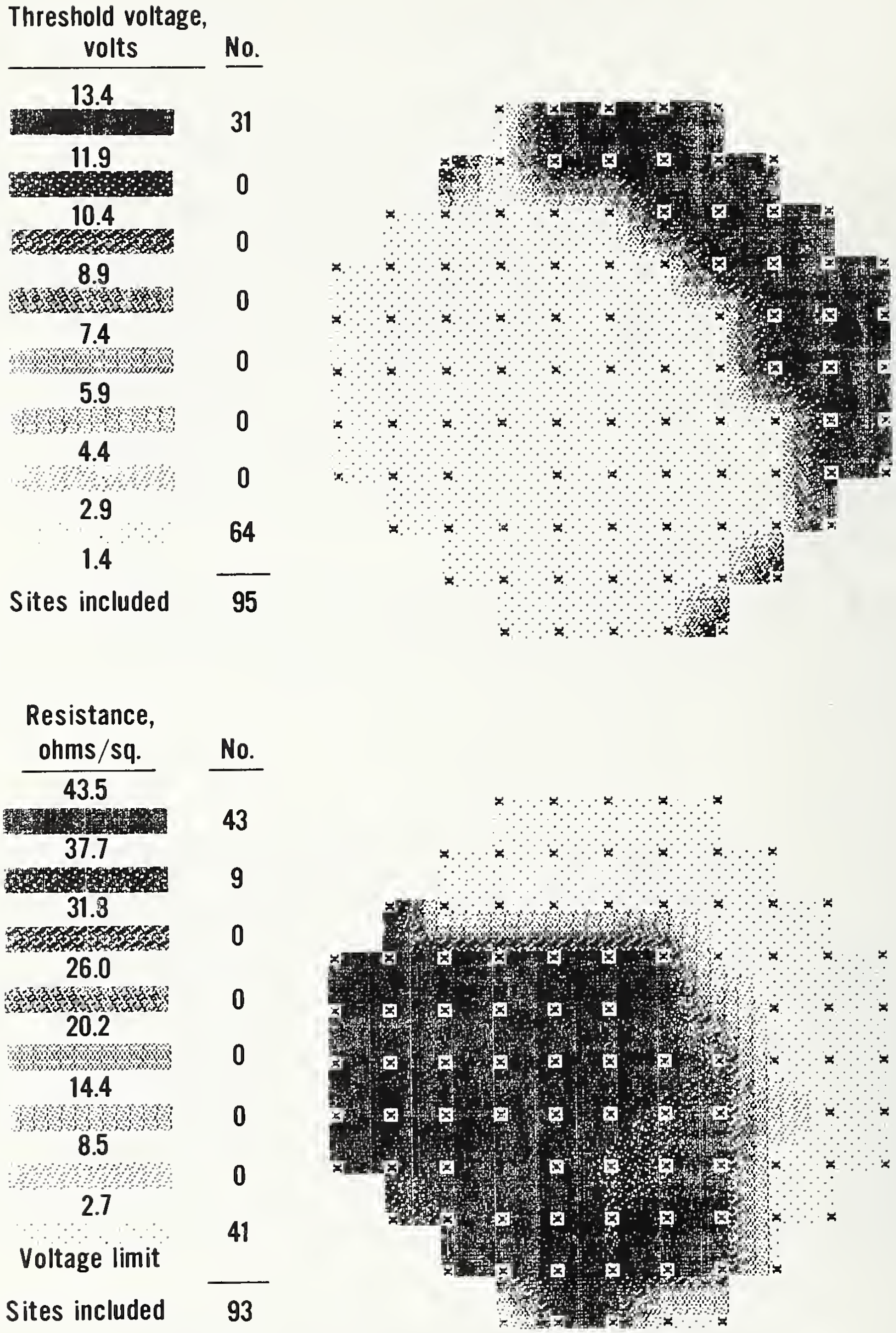


Figure 10. Wafer maps showing location of nonfunctional *n*-channel MOSFETs (top) and n^+ sheet resistor test structures (bottom) for NBS-26 PVW B4.

measurement, a current is forced through two adjacent taps of the structure, and voltage is measured at the two remaining taps. Sheet resistance is then calculated from the voltage measured for a fixed current in the structure. When electrical contact is not made to the structure, no voltage is measured between the voltage taps, and the calculated sheet resistance is approximately zero.)

Based on these data, it was possible for the manufacturer to isolate the source of the processing problem to that portion of the process between contact window lithography and metallization deposition. Further evaluation by the manufacturer revealed that a change in a premetallization chemical cleaning procedure had occurred and that contamination was being introduced during one of the wafer drying steps.

5.2 Random Fault Test Structure Evaluation

A random fault test structure is a microelectronic structure which can be electrically tested in order to determine the density of certain types of faults associated with the fabrication process [9]. These structures usually consist of arrays of identical elements connected electrically in a series, parallel, or addressable configuration. Two types of developmental random fault test structures were included on NBS-16 and NBS-26.

The purpose of using a random fault test structure on a test pattern is to provide the user and manufacturer with a tool which can be used to assess the yield potential and identify the principal yield detractors associated with the process being used. For the manufacturer, test results can be used to identify, quantify, and correct yield-limiting processes in the fabrication process. For the user, test results can be used to monitor the manufacturer's performance with time, rate the performance of multiple manufacturers, or accept or reject products.

Several factors must be considered before selecting and using a random fault test structure. Briefly, they are:

(a) What type of structure should be used? If the structure selected does not provide information about principal fault mechanisms in the process, test results and analysis will be of little use in improving yield.

(b) What size should the structure be? If a series or parallel type of array is used and the array size is too large, all arrays will probably contain at least one fault. On the other hand, if the array size is too small, a single array has a high probability of containing no faults. If a large number of small arrays is employed, testing time and probing difficulties increase. The array size for a single structure must be selected such that enough faults will be detected that some form of statistical analysis can be performed.

(c) Is the fault detected the intended fault? If a structure were used to detect dielectric faults in capacitor arrays and serious metallization bridging between interconnect lines from probe pads to the capacitors occurred, a fault would be detected, but the identity of the fault would be incorrect.

(d) Is the fault detected a singular fault or a clustered fault? If, for instance, a continuity test is performed for a metallization interconnect and test results indicate a break, is the break at one location? Two? Ten?...

(e) What degree of testing complexity and time is required to obtain meaningful information? If the time required to test and evaluate the structure is too great to provide timely information to the fabricator, the structure will be of little value.

One of the two random fault structures included on NBS-16 and NBS-26 is a new type of developmental fault structure which can both provide information on a variety of faults common to MOSFET devices and in general determine the location of the faults. The other structure, an MOS capacitor array, is a more conventional parallel array intended to determine the occurrence of gate dielectric failure at the epi island edge.

5.2.1 Random Access Fault Structure (RFI)

The purpose of including this type of structure on NBS-16 and NBS-26 was to develop a general purpose random fault structure which can be used to detect, identify, and evaluate faults common to MOSFET structures without foreknowledge of dominant fault type or fault density. The structure is a random access structure which allows one to identify different fault types and determine the exact location of the fault for further analysis. One can determine if the fault is singular or clustered and also obtain parametric electrical data which can be used in further analysis. In Area III, each NBS-16 test pattern contains four of the random access fault structures, shown in figure 11. The top two are *p*-channel; the bottom two are *n*-channel. Each structure contains a 10 by 10 array of minimum geometry MOSFETs. There are 400 MOSFETs per pattern and thus a total of 38,000 MOSFETs on the 95 sites of each PVW. Within each array, each MOSFET has the gate electrically tied to drain. The devices are arranged in rows and columns similar to a diode matrix. Each MOSFET is isolated from its neighbor and can be individually addressed by selecting the appropriate row and column probe pads as shown in figure 12. The vertical columns are made of metal, the rows of polysilicon. Each MOSFET has a gate size of 0.2 by 0.6 mil (5.1 by 15.2 μm). Testing is accomplished in two phases with the automatic computer-controlled test system. The first phase, a row-to-row and column-to-column integrity test, is to establish whether there is electrical conductivity between adjacent rows or columns. If the structure passes this test, each MOSFET is individually tested to determine the threshold voltage measured at 1-μA source-to-drain current, the source-to-drain breakdown voltage measured at 10-μA source-to-drain current, and the source-to-drain leakage current measured with the gate and drain grounded and source held at 10 V. These data and site location are recorded.

To evaluate the data, failure criteria must first be established. For this work, two criteria were recommended by the manufacturer as limits which, if exceeded, would result in circuit failure. They are:

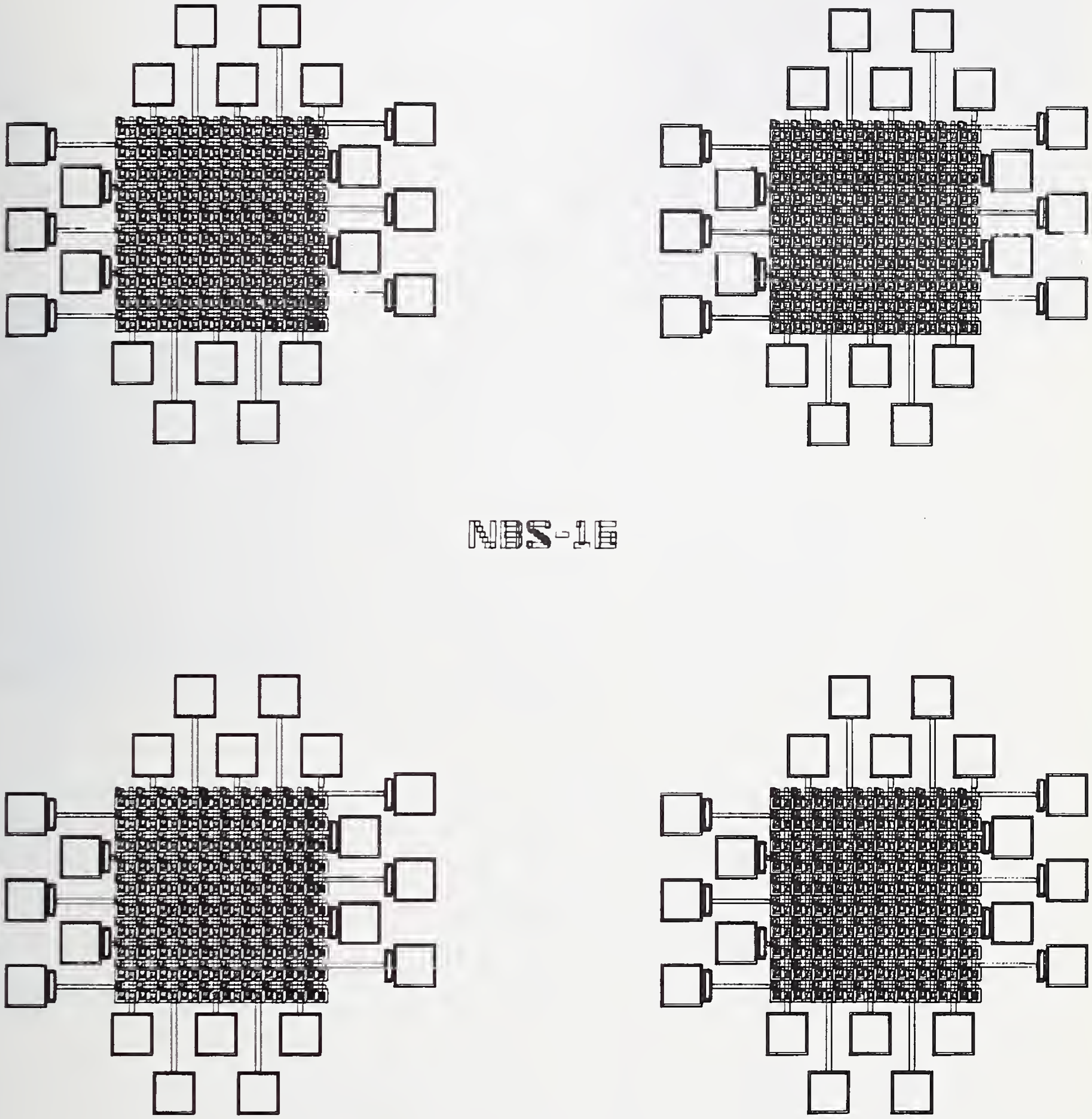
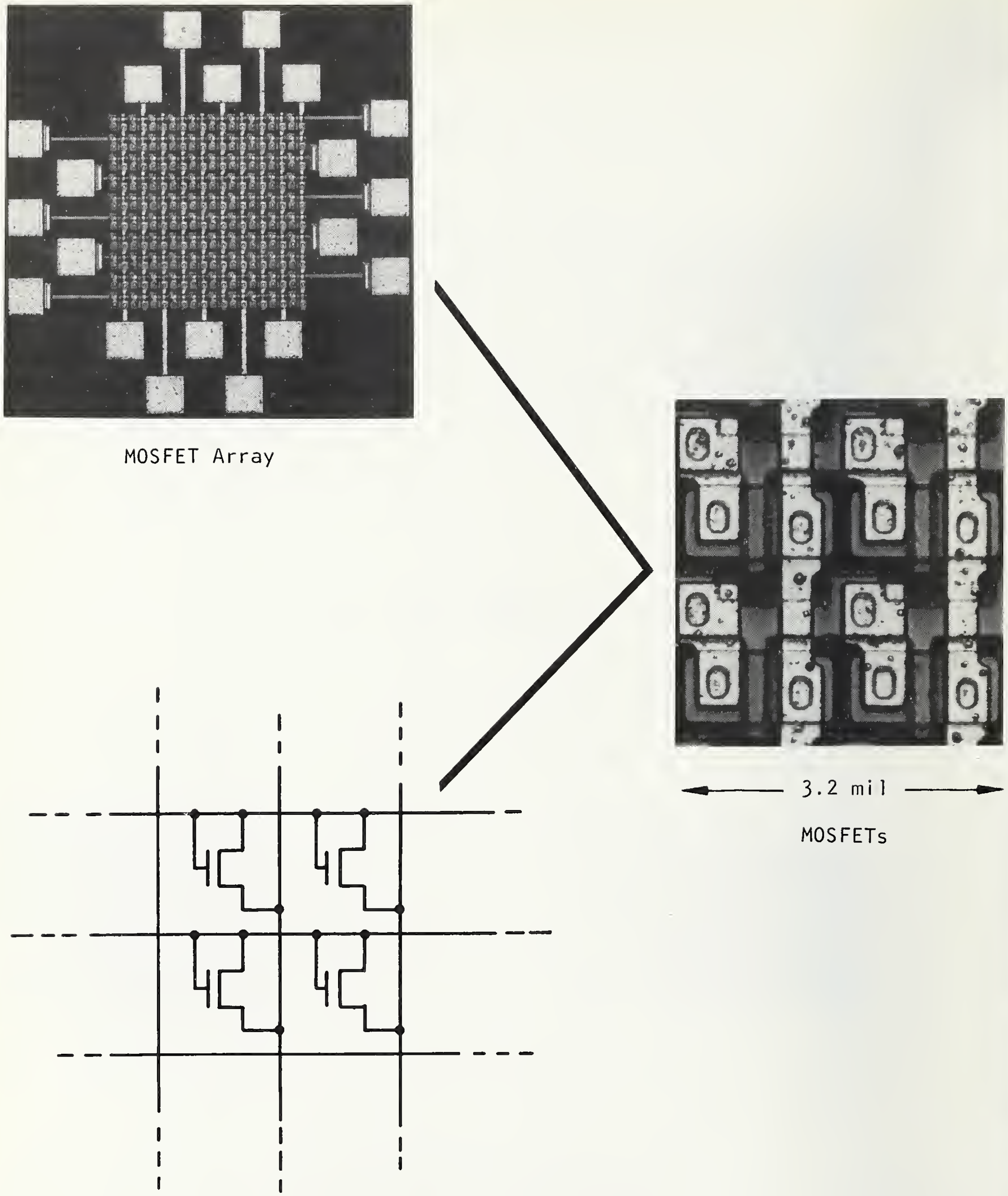


Figure 11. Random access fault structure, RFI, contained on one NBS-16/26 test pattern. Top, two arrays p-channel MOSFETs; bottom, two arrays n-channel MOSFETs.



Electrical Interconnect

Figure 12. One random access fault structure RFI, showing a micrograph of a two-by-two section of MOSFETs and a schematic of the electrical interconnect.

(a) a source-to-drain leakage current greater than 50 nA/mil (2 nA/μm) gate width, and

(b) a source-to-drain breakdown voltage less than 17 V or greater than 30 V. (This upper limit was an arbitrary bound to enable one to determine when the voltage compliance limit of the current supply was reached.)

A third criterion was also used. A MOSFET was considered to have failed if the threshold voltage was above or below a preselected bound. This bound can be determined from circuit simulation programs or past experience. Since no data were available from these sources on which more precise bounds could be established, the following criterion was used:

(c) A MOSFET was considered to have failed if the threshold voltage was outside the four-sigma limit where sigma is the sample standard deviation of the data from test results of discrete MOSFETs tested in the process parameter pattern. The threshold voltage data sample was assumed to follow a Gaussian distribution, and data falling outside this distribution were considered to be failures. For a population of approximately 25,000 independent samples, only a single valid datum was expected to fall outside this limit.

Figure 13 is a graphical presentation of the outcome of the test results of one array. By analyzing the test results and comparing the outcome of individual sites to the nearest neighbors, the exact fault location and the category of fault type can be determined. Examples of this are shown in figure 13. Visual inspection was used to confirm the indicated break in metallization and the dielectric gate short. By testing a large number of these arrays, a variety of different electrical fault types can be identified. These fault types can be separated into two basic groups: physical faults and parametric faults.

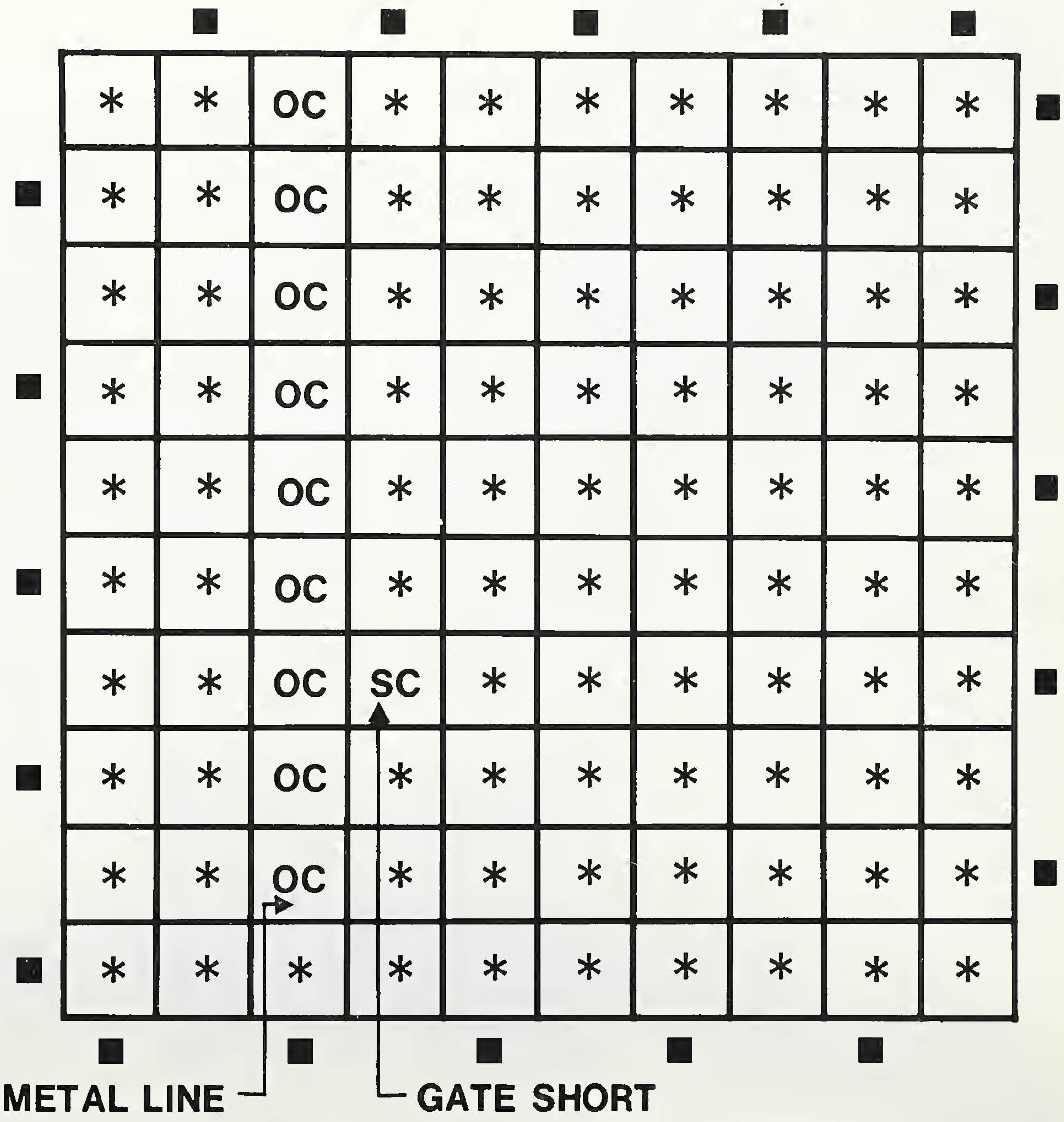
Physical faults are those which produce a definite physical failure which directly results in circuit failure. Examples are: poly, metal, or epi voids or breaks; poly, metal, or epi bridges; contact window opens; gate dielectric shorts; and poly or metal step coverage breaks. A parametric fault or parametric variation outside a predetermined bound may or may not produce a circuit failure. Examples of parametric failures are a high source-to-drain leakage current or low source-to-drain breakdown voltage. Failures caused by either physical or parametric faults may or not be visible.

Test results from the random access fault structure on PVWs accompanying product lots A6 and A1 are shown in figures 14 and 15, respectively. For these two lots, the product being manufactured consisted of a circuit containing about 5,000 transistors. PVW A6 accompanied a product lot which had a wafer probe yield nine times greater than the product lot accompanying PVW A1. Test results from test patterns on the interior 67 sites within the PVW are presented.

The detection of fault location is important because it provides information about how the faults are distributed over the area being tested. For a given number of faults, a nonuniform fault distribution generally results in a

MEMORY-LIKE RANDOM FAULT TEST STRUCTURE RESULTS FOR ONE ARRAY

- * PARAMETERS WITHIN NORMAL LIMITS
- OC OPEN CIRCUIT
- SC SHORT CIRCUIT
- ■ PROBE PAD LOCATION



*	*	OC	*	*	*	*	*	*	*
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*	*	OC	*	*	*	*	*	*	*
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*	*	OC	*	*	*	*	*	*	*
*	*	OC	SC	*	*	*	*	*	*
*	*	OC	*	*	*	*	*	*	*
*	*	OC	*	*	*	*	*	*	*
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Figure 13. Test results for one RFI array from NBS-16 PVW A1.

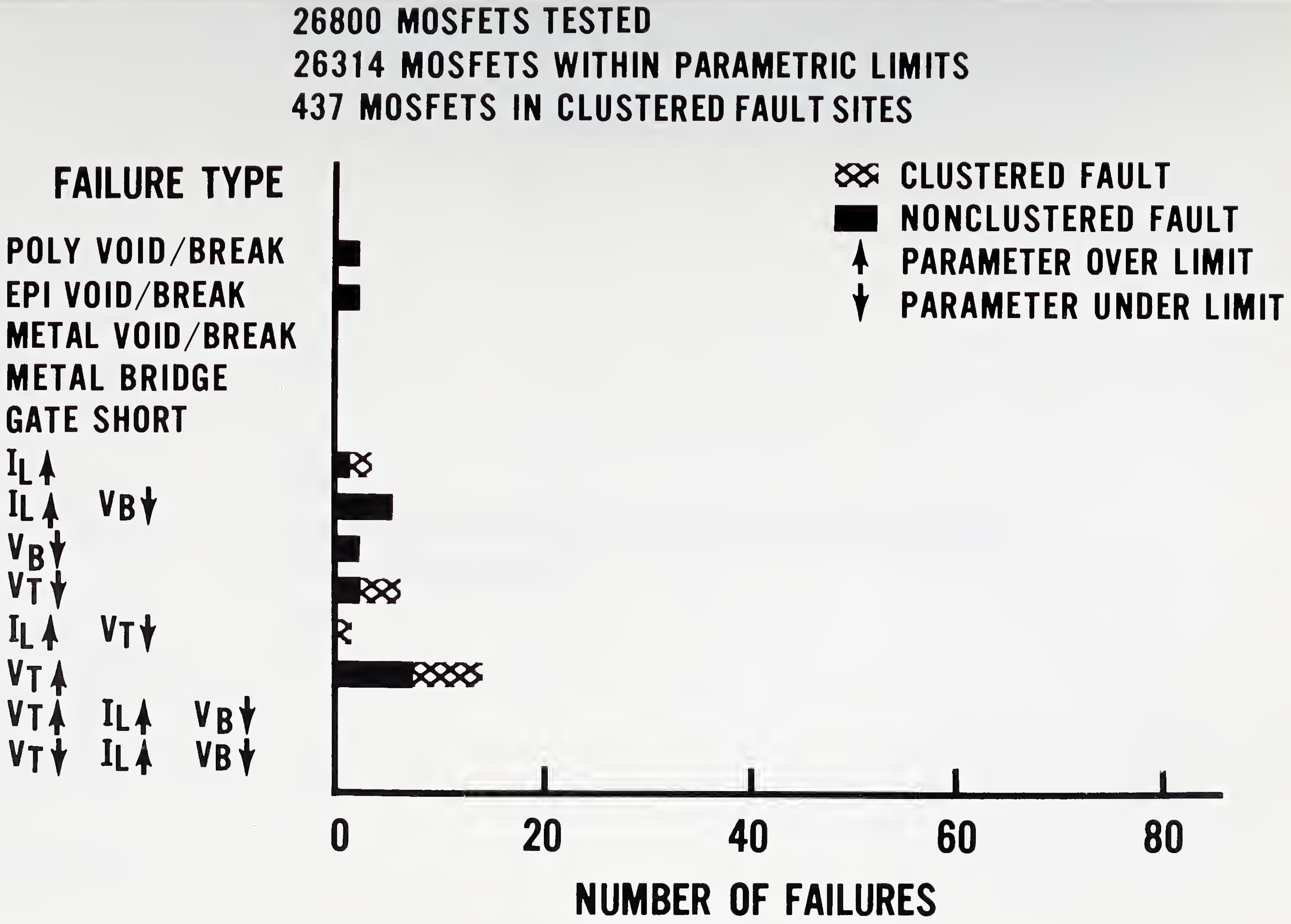

Figure 14. Test results for 268 RFI structures from NBS-16 PVW A6 (where I_L is source-to-drain leakage current, V_B is source-to-drain breakdown voltage, and V_T is threshold voltage).

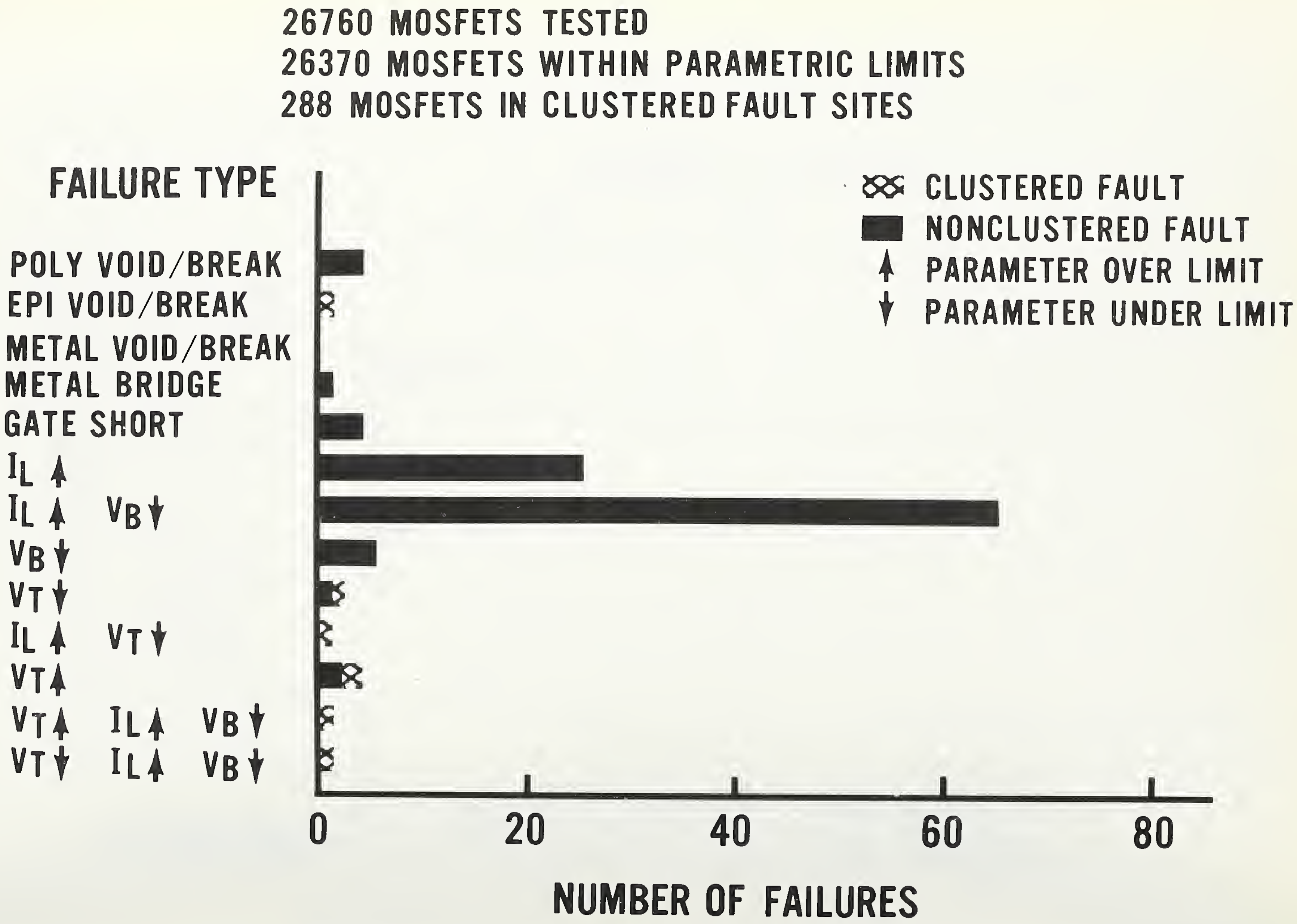

Figure 15. Test results for 268 RFI structures from NBS-16 PVW A1 (where I_L is source-to-drain leakage current, V_B is source-to-drain breakdown voltage, and V_T is threshold voltage).

higher potential product yield as all of the faults tend to be located in a relatively few product sites. A more uniform fault distribution generally results in more product sites containing a fault and therefore a lower product yield. A more detailed description of the effects of fault distribution on product yield can be found elsewhere [10].

A fault is clustered when two or more adjacent transistor failures of the same or similar type are detected within an array. When this occurs, the entire cluster is counted as one clustered fault. As may be seen in figure 14, information on both clustered and nonclustered faults for PVW A6 is presented; however, few failures of either category were detected. Data for both *p*- and *n*-channel MOSFETs are plotted together. Based on these test results, it was possible to eliminate certain failure mechanisms as the principal cause of yield degradation. For example, no gate-to-source shorts were detected. Also, metallization coverage can be considered good. To test 26,800 MOSFETs required that 107,200 metallization steps be covered. Further testing at higher current levels confirmed the electrical quality of the step coverage.

Test results from PVW A1 indicate the presence of a major yield-limiting fault type. The dominant fault detected is a nonclustered, parametric type fault. Eighty-seven out of 26,700 MOSFETs evaluated had a source-to-drain breakdown voltage or both a source-to-drain leakage current and breakdown voltage which fell outside one or more of the previously described failure criteria. Since the number of faults detected was approximately the same for both *p*- and *n*-channel MOSFETs, test results for both types are plotted together.

A histogram of breakdown voltage for all devices with a source-to-drain leakage current greater than the failure criterion is shown in figure 16. The distribution is peaked at about 14 to 15 V. In most cases, leakage current was much greater than the 50 nA/mil (2 nA/μm) of gate width failure criterion.

Because the location of each fault was known, selected MOSFETs were inspected; however, no visible defects were observed. When individually tested, the MOSFETs exhibited noisy soft breakdown characteristics. Figure 17 is a wafer map showing the approximate location of the faults that were detected by this technique.

This type of failure seems to be run-dependent, since test results from PVW A6 do not indicate a large number of these faults. At this time, further physical analysis is required to determine the exact nature and physical cause of this defect.

To summarize, by using a random access fault structure, it was possible to identify a yield-limiting fault which was unknown to the manufacturer and user at the time of test structure design and selection. The location of each fault could easily be determined from the test results. The dominant fault encountered had electrical characteristics with lower-than-normal source-to-drain breakdown voltage, with a mean of approximately 14 V, a source-to-drain leakage current greater than 50 nA/mil (2 nA/μm) of gate

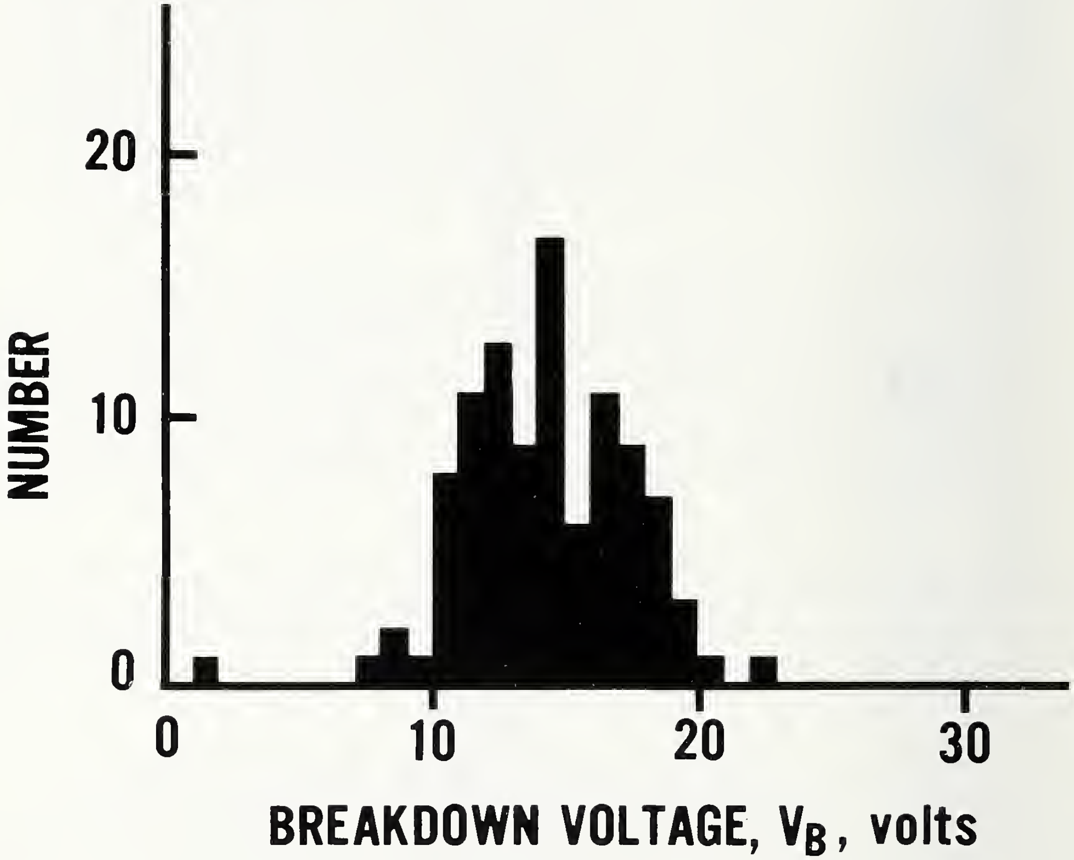

Figure 16. Histogram of breakdown voltage, V_B, volts, with devices with a source-to-drain leakage current greater than 50 nA/mil (2 nA/μm) gate length for NBS-16 PVW Al.

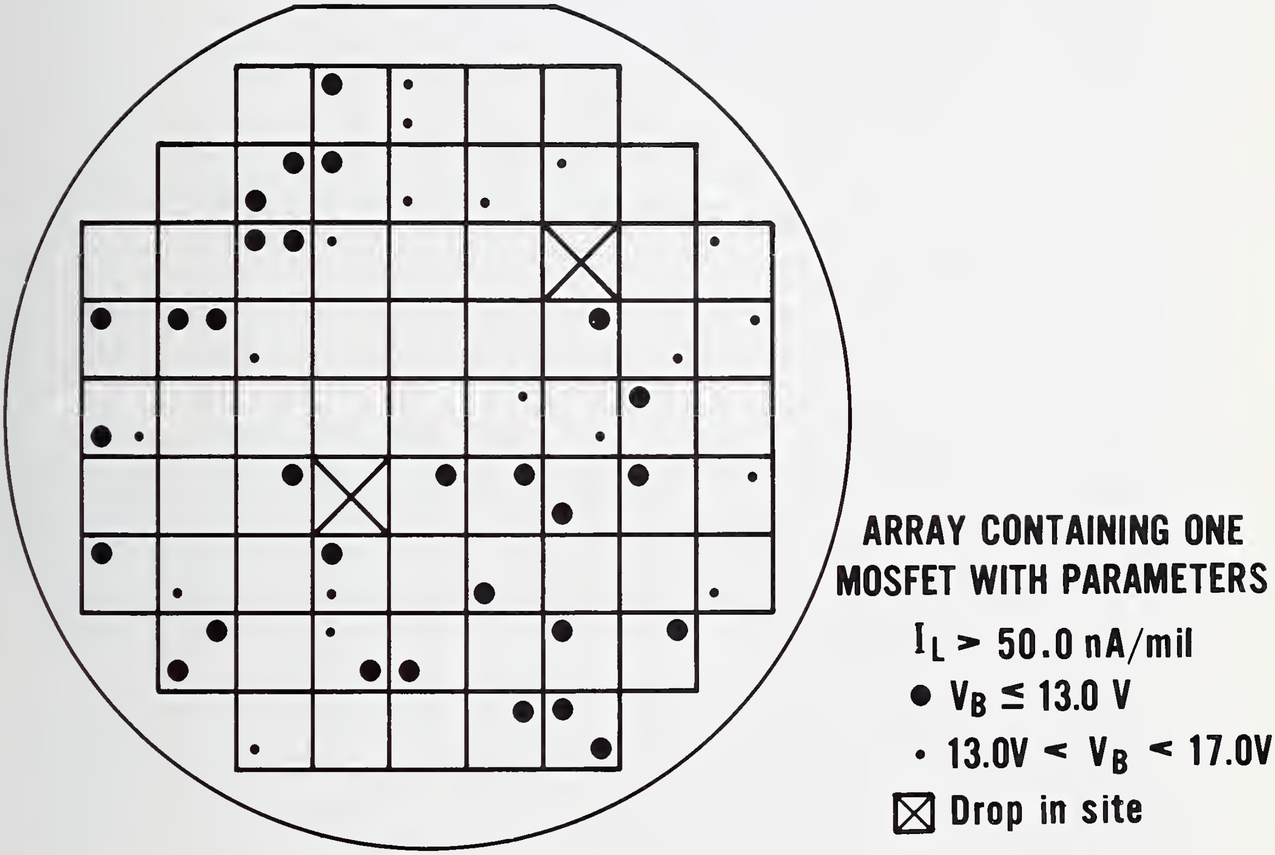

Figure 17. Failure map showing approximate location of RFI structures containing MOSFETs with high source-to-drain current leakage.

width, and was not clustered. Also, no visible defects were observed at each fault location.

The random access fault structure is important for two reasons. First, it has been demonstrated that test results can be used to identify the exact location of each fault. Further electrical or physical analysis can then be undertaken. Second, the random access fault structure is able to identify different fault types. In one example, a major fault was detected that had not been previously anticipated; this fault would not have been detected from the other test structures included on the pattern. The random access fault structure was able to provide test results that allowed the determination of the relative fault density and relative ranking of different fault types. The user and manufacturer can use this structure as a tool to identify the major yield-limiting process problems affecting their process.

5.2.2 Gate Dielectric Integrity Array (RFII)

The purpose of including this type of random fault test structure on NBS-16 and NBS-26 was to develop and evaluate a structure which could be used to analyze one particular type of physical and electrical defect common to MOSFETs made in an SOS technology, namely, gate dielectric leakage from poly-to-epi island occurring through the gate oxide at the epi-island edge. The structure was designed such that metal-to-poly and metal-to-epi leakage could also be detected.

The approach taken was to design a parallel array type of random fault test structure consisting of subarrays of identical capacitor elements. Each subarray was then electrically tested and the results compared to a failure criterion. From these results, the yield (the ratio of the number of good subarrays to the total number of subarrays tested) could be determined for each subarray size. Similar types of structures have been described by others [9].

The gate dielectric integrity array, RFII, is shown in figure 18. The structure occupies Area IV of the test pattern. It contains capacitor arrays which can be used to detect poly-to-epi leakage caused by dielectric defects in the gate oxide. It can also be used to measure photolithography-induced defects or dielectric defects in the field oxide by detecting leakage between metal-to-poly and metal-to-epi levels. The structure is comprised of five layers on a sapphire substrate: n^- epitaxial silicon; gate oxide; p^+ polysilicon; field oxide; and aluminum metallization. The poly lines are grouped to form seven subarrays with 57, 114, 225, 375, 750, 1500, and 3000 crossovers. The polysilicon and metallization in each subarray are each connected to a single probe pad; all of the epi lines in all of the subarrays are electrically common and connected to a single probe pad.

The size of the entire structure and the sizes of the subarrays were selected as an arbitrary compromise between maximizing the number of elements (capacitors) from which a statistically significant data base can be obtained and minimizing the overall size of the structure to one that could be reasonably included within the test pattern. There are 95 RFII structures on each PVW. Each structure is in a 100-mil (2.54-mm) square and can be probed by means of a 2 by 10 probe card.

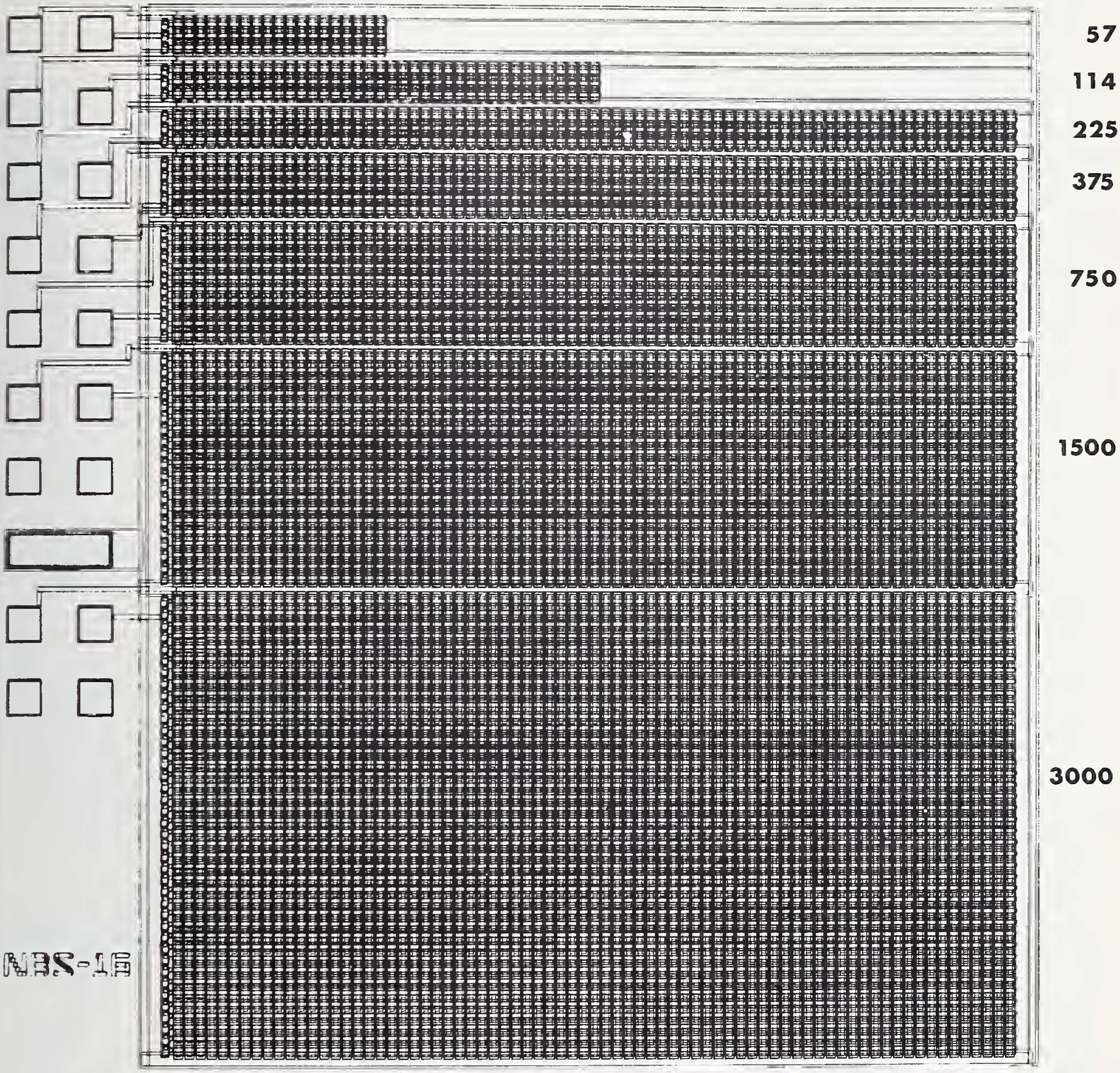

Figure 18. Gate dielectric integrity array, RFII. The number of elements for each subarray is listed at the right.

For each structure, a probe-to-probe-pad continuity is first made on the two common probe pads shown in figure 18. The use of only one set of common probe pads for determining electrical continuity places a limitation on the overall usefulness of the test structure as designed. Double probe pads for each subarray would ensure that electrical continuity is established and that a test result indicating no current leakage is the result of the oxide integrity of the subarray being tested and not probe-to-probe-pad misalignment. Use of double probe pads does increase the area required for the test structure and the time required for automatic testing.

For the present structure, however, if continuity is established at the two common probe pads, it is necessary to assume that probe-to-probe-pad continuity exists for the entire 2 by 10 probe-pad array. Each subarray is then individually tested by applying 10 V between the poly and epi contacts and measuring any detectable leakage current. Similar testing procedures are also followed to determine leakage between metal-to-poly and metal-to-epi subarrays. Also, a series of tests is performed to determine the leakage between the electrical nodes of the different subarrays. Data are recorded on a floppy disc for later evaluation.

The primary advantage of using this type of structure is that the time required to test a large number of elements is very small since large parallel arrays can be tested by one or two measurements. The structure is also useful in that it addresses primarily one type of fault.

The primary disadvantage of using this type of structure is in evaluating the test results obtained and in determining meaningful statistical results. One reason for this is that the structure cannot identify the occurrence of more than one fault in a particular subarray. However, the two major sources of difficulty are: (1) defining the magnitude of leakage current necessary to consider the subarray to have failed and (2) separating electrical interferences between adjacent subarrays occurring from the presence of unintended faults.

Test results from RFII structures on the PVW accompanying lot A6 are shown in figure 19. The yield of the structure is plotted as a function of the number of elements tested. Any array with a leakage greater than 1.0 μA was considered to have failed.

The bands accompanying the curve are the uncertainty of the measurement introduced by interferences caused by the test structure. An example of a typical interference is the occurrence of an unintended fault causing electrical communication between two adjacent subarrays. A typical example of this type of unintended fault is a poly bridge or a metallization bridge electrically linking two subarrays. When an unintended fault is detected for a subarray pair and an intended fault is detected for that combination, an uncertainty arises as to which subarray contained the fault or if both subarrays contained a fault. The upper and lower bounds of the curves in figure 18 represent the highest yield and lowest yield, respectively, that can be determined from test results where unintended faults are present.

Lowering the leakage current failure threshold criterion greatly increases the uncertainty associated with evaluating the test results. As can be seen

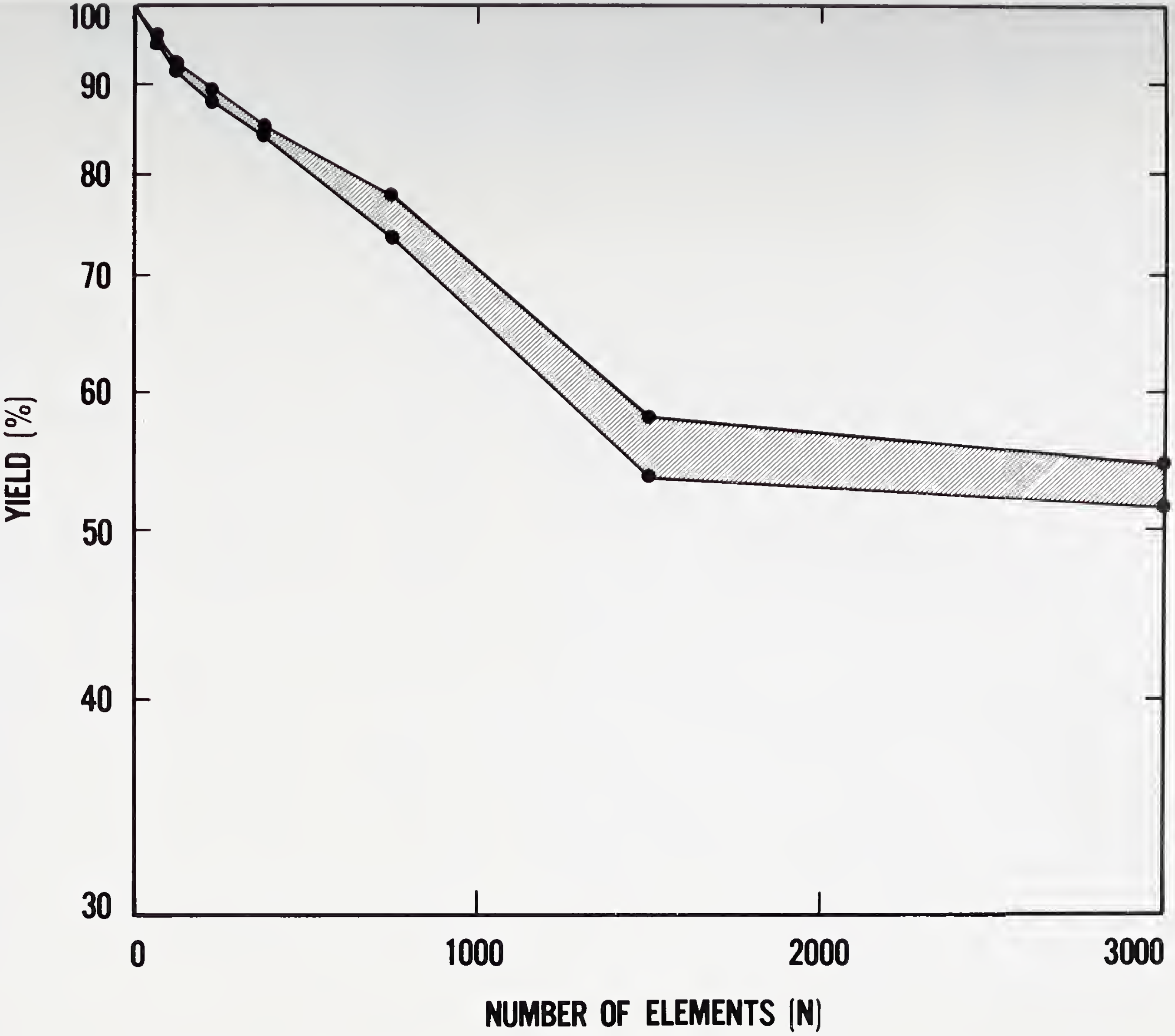

Figure 19. Yield *versus* number of elements tested from NBS-16 PVW A6 with a leakage current greater than 1.0 μA at 10 V. Wafer probe yield of product accompanying PVW was 5.4 percent.

in figure 20, if the failure threshold is lowered to 10^{-4} μA, the uncertainty bands increase.

Test results from RFII do allow for some basis of yield evaluation. If the yield *versus* number of elements, N, were extrapolated to an N of 5000 in figure 19, the resultant yield predicted would be considerably greater than the product yield measured. Given the accuracy of the test structure measurements and accompanying uncertainty, this suggests that the principal source of yield degradation is not breakdown of the dielectric layers which separate the episilicon, polysilicon, and metallization.

In order to improve the accuracy of these results, the structure should be redesigned with greater separation between subarrays. This would reduce the possibility of metal or poly bridging between subarrays. Also, the structure should be designed such that only one fault type can be detected. For instance, a structure intended to detect poly-to-epi faults should consist of poly-over-gate-oxide-over-epi layers only. The absence of metal will remove the possibility of electrical interferences by combined metal-to-epi and metal-to-poly shorts. These steps will increase the area required for a structure and eliminate the possibility of detecting metal-to-poly and metal-to-epi faults. Also, the use of double probe pads for the entire structure will ensure that probe-to-probe-pad continuity is established for each subarray. To establish a more meaningful correlation between the test results from RFII and product yield, a precise estimate of the poly-to-epi leakage current required to cause circuit failure must be available. This estimate must come from circuit modeling work.

Use of random fault test structures consisting of parallel or series arrays of identical elements can be a valuable method of acquiring test results from a statistically significant data base from which yield estimates can be made. Testing time and equipment are minimal. Care must be taken in structure design and selection to ensure that:

(a) the occurrence of unintended faults is minimized or that they can readily be identified,
(b) well-defined failure criteria exist, and
(c) the fault being detected represents a dominant fault mechanism occurring in the process.

6. CONCLUSIONS

6.1 Process Parameter Pattern

In order to be able to characterize the performance of integrated circuits, it is necessary to determine first the baseline electrical parameters of the process. The data presented show that significant variations in these parameters can occur across a wafer and from wafer lot to wafer lot. In order to obtain reasonable estimates of these parameters, it is insufficient merely to measure two or three test structures per wafer, as is often done, and expect an accurate result. A large sample of test sites must be available in order to make a statistically significant estimate of the desired parameter.

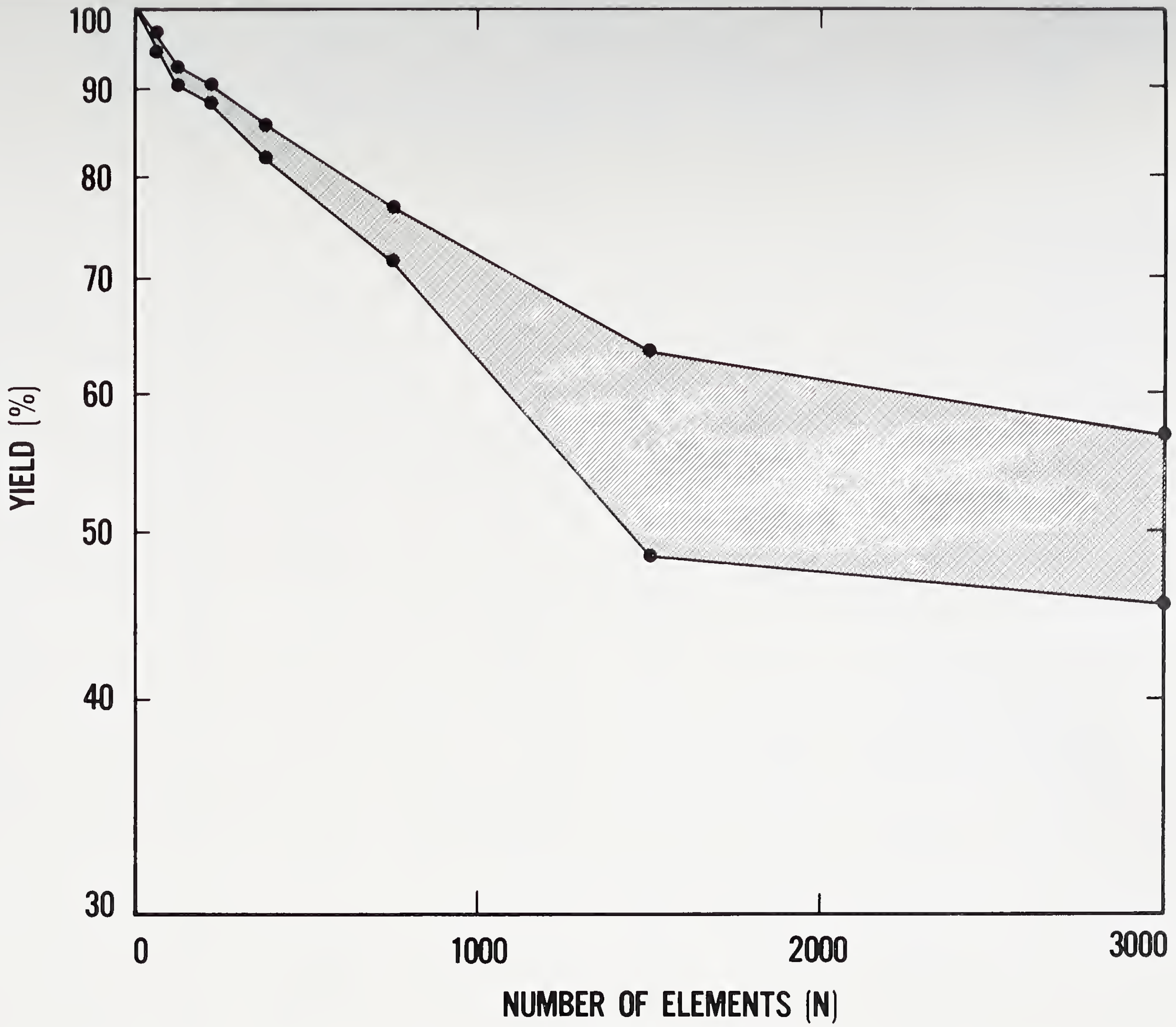

Figure 20. Yield *versus* number of elements tested from NBS-16 PVW A6 with a leakage current greater than 1.0 × 10^{-4} μA at 10 V.

As can be seen from the wafer maps presented, the mean, median, and standard deviation are not necessarily sufficient information on which to fully evaluate electrical characteristics. For instance, the linewidth variation for the p^+ cross-bridge sheet resistor for PVW A9 as seen in figure D-19 of Appendix D appears very uniform over the wafer and can be adequately characterized by statistical parameters. Conversely, examples previously given in this report illustrate examples where intrawafer variations do occur and can be used for parameter correlation. In either case, sufficient data must be taken and wafer maps produced in order to determine if the parameters are uniformly distributed over the wafer or a pattern exists. Graphical parameter mapping techniques provide an important tool for making correlations of critical parameter variations and identifying process problems which cannot be detected by other means. Much of the data and analyses presented identified process irregularities which were unknown to the manufacturer.

How many test sites are enough? This question cannot be directly answered, but must involve the judgment of the user and manufacturer and the maturity of the process being used. For a new developmental process, the identity, spatial variation across a wafer, and the reproducibility of critical process parameters must first be determined. A reasonable approach for determining this is to run process lots of wafers containing only test patterns. As the process matures and sufficient confidence exists, a PVW can be used in conjunction with test pattern "drop-ins," test patterns substituted for the product at selected sites on a product wafer, to monitor critical parameters. Finally, for a mature process in which all parameters are well controlled and the product completely testable, the use of test patterns can be minimized as the product yield itself becomes the measure of process control. As chip complexity increases and the possibility of complete functional testing of VLSI circuits diminishes, test patterns may provide the only means of assessing process performance.

6.2 Random Fault Test Structures

Two types of random fault test structures were included on NBS-16 and NBS-26: a random access fault structure (RFI) and a gate dielectric integrity array (RFII).

Test results from RFI show that the identity and location of failure mechanisms can be detected by an addressable array and that a relative fault density of different failure mechanisms introduced during the fabrication process can be determined with this structure. This type of structure is important because it does not require the user or manufacturer to have foreknowledge of the major faults that may be encountered in a process. Further work is necessary to increase the size of random access fault structures and to minimize the testing time per element. The gate dielectric integrity array is a random fault test structure which can be tested quickly; it provides information about one specific type of fault. The effects of interferences caused by unintended faults can be reduced through improvements in the design of the structure.

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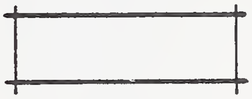
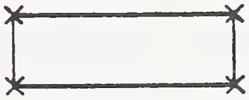
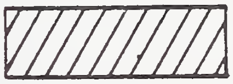
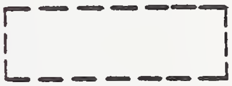
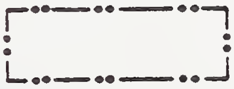
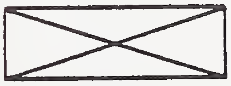
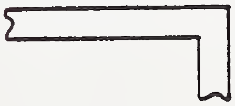
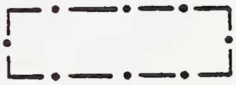
Appendix A

NBS-16 AND NBS-26 TOPOLOGICAL DESIGN RULES

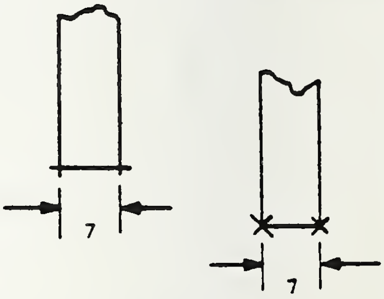
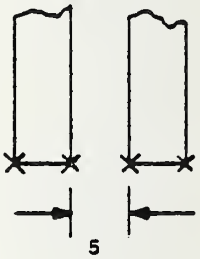
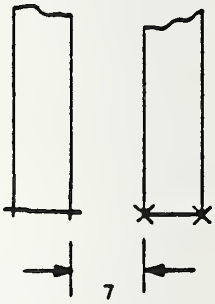
The following design rules were used for test structure layout. They are taken from Manufacturing Technology for Radiation-Hardened Microprocessor, Interim Technical Report No. 4, by J. J. Fabula, M. G. Kane, and D. S. Woo, and are reproduced with the permission of the Air Force Wright Aeronautical Laboratory.

RADIATION HARDENED CMOS/SOS DESIGN RULES (P^+ POLYSILICON)

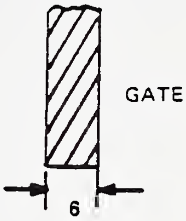
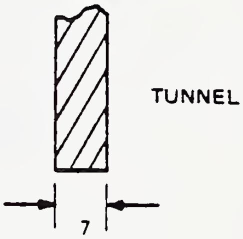
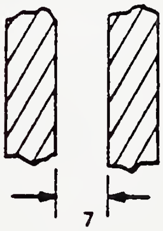
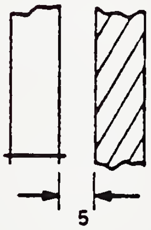
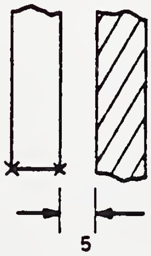
Mask Level	Mask Designation	Street	Symbol
Level 8: Epi Islands	ILD	No	
NMOS Island	—	—	
PMOS Island	—	—	
Level 3: Polysilicon	PLY	No	
Level 4: n^+ Diffusion Level $\overline{4}$: n- Diffusion (Reverse Tone of Level 4)	N^+	No	
Level 9: p^+ Diffusion	P^+	No	
Level 5: Contact	CNT	Yes	
Level 6: Metal	MET	No	
Level 7: Bond Pad	PAD	Yes	

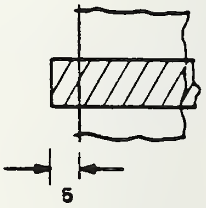
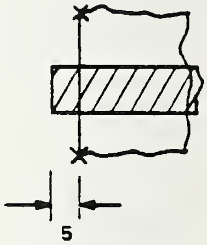
1. *Minimum Values*

a. Level 8: Epi Islands

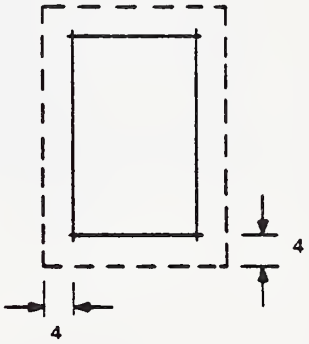
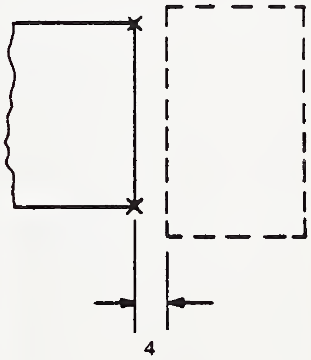
Rule #	Item	Minimum Value µm (mil)	Illustration Value (µm)
8.1	Width of NMOS Island	7 (0.28)	
	Width of PMOS Island	7 (0.28)	
8.2	Spacing, NMOS Island to NMOS Island or PMOS Island to PMOS Island	5 (0.2)	
8.3	Spacing NMOS Island to PMOS Island	7 (0.28)	

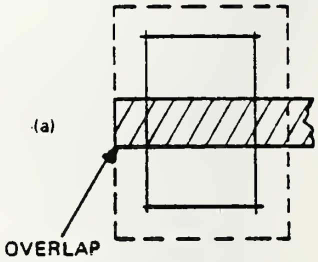
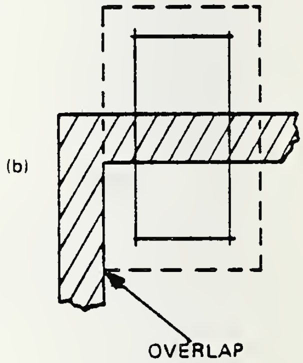
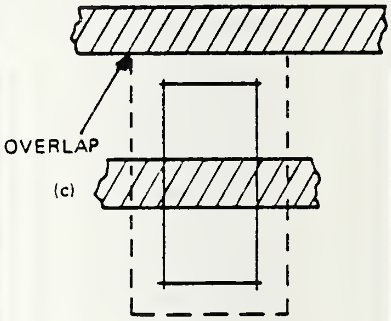
b. Level 3: Polysilicon

Rule #	Item	Minimum Value µm (mil)	Illustration Value (µm)
3.1	Width of Polysilicon Gate	6 (0.24) 5 (0.20)	
3.2	Width of Polysilicon Tunnel for Interconnection	7 (0.28)	
3.3	Spacing, Polysilicon to Polysilicon	7 (0.28)	
3.4	Spacing, Polysilicon to NMOS Island	5 (0.2)	
3.5	Spacing, Polysilicon to PMOS Island	5 (0.2)	

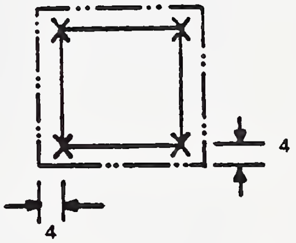
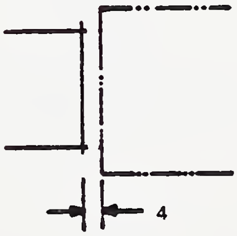
Rule #	Item	Minimum Value µm (mil)	Illustration Value (µm)
3.6	Polysilicon Extension Beyond NMOS Island	5 (0.2)	
3.7	Polysilicon Extension Beyond PMOS Island	5 (0.2)	

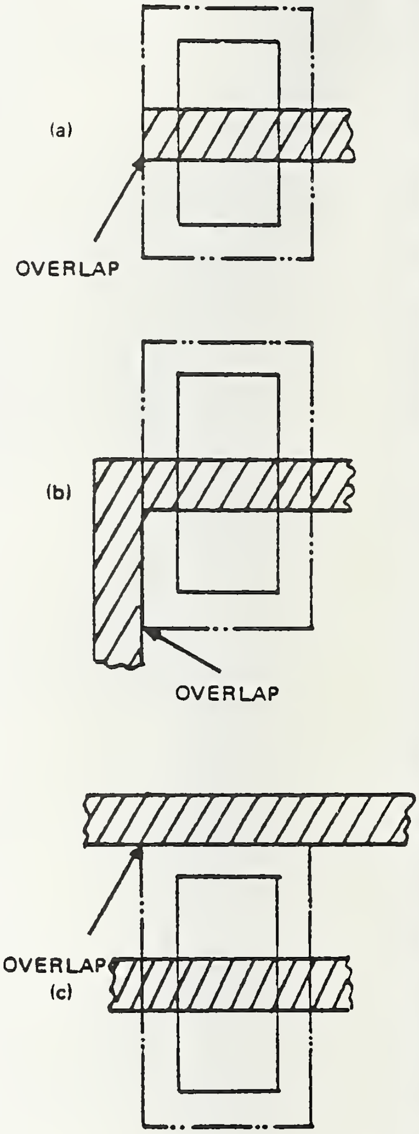
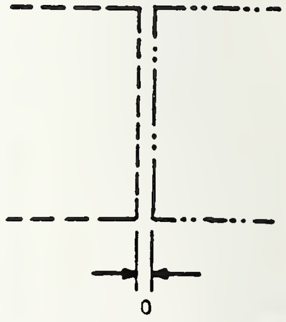
c. Level 4: n^+ Diffusion

Rule #	Item	Minimum Value µm (mil)	Illustration Value (µm)
4.1	Overlap, n^+ Diffusion to NMOS Island	4 (0.16)	
4.2	Spacing, n^+ Diffusion to PMOS Island	4 (0.16)	

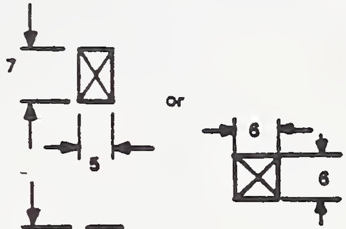
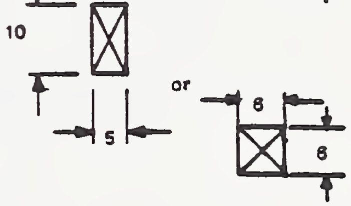
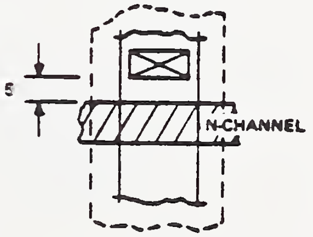
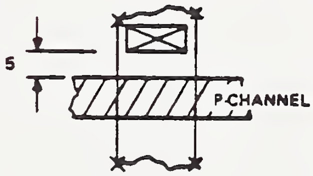
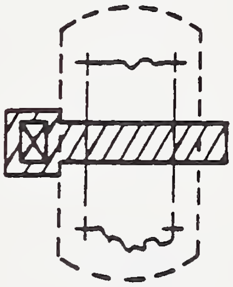
Rule #	Item	Minimum Value μm (mil)	Illustration Value (μm)
4.3	Overlap of n^+ Diffusion and Polysilicon is allowed	0	  
NOTE	This does NOT exempt the designer from following rules 3.6 and 3.7. Minimum polysilicon extension is 5 μm (0.2 mil)		

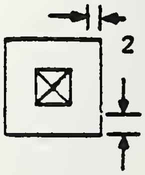
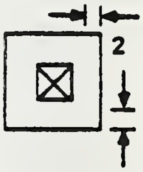
d. Level 9: p^+ Diffusion

Rule #	Item	Minimum Value µm (mil)	Illustration Value (µm)
9.1	Overlap, p^+ Diffusion to PMOS Island Exception: To achieve substrate strapping, a portion of the PMOS island may be outside the p^+ diffusion.	4 (0.16)	
9.2	Spacing, p^+ Diffusion to NMOS Island	4 (0.16)	
9.3	~~Overlap, p^+ Diffusion to n^+ Diffusion for Zener Diode~~ Zener Diodes NOT Allowed		

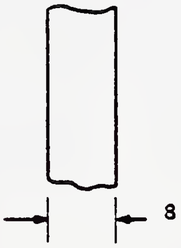
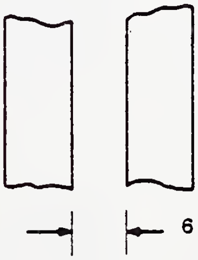
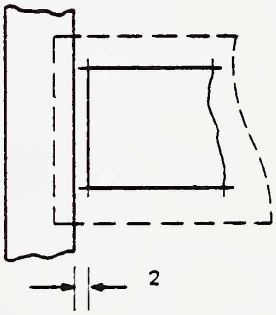
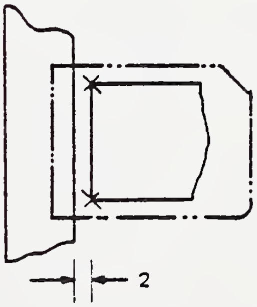
Rule #	Item	Minimum Value μm (mil)	Illustration Value (μm)
9.4	Overlap of p^+ Diffusion and Polysilicon is allowed	0	
NOTE	This does NOT exempt the designer from following rules 3.6 and 3.7. Minimum polysilicon extension is 5 μm (0.2 mil)		
9.5	Spacing of p^+ to n^+ Diffusion (coincidence is allowed)	0	

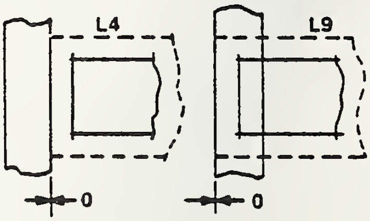
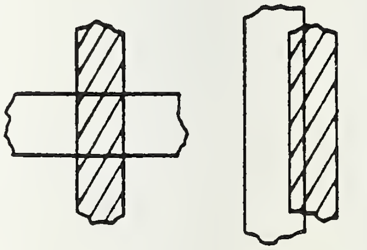
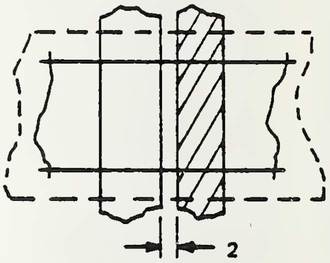
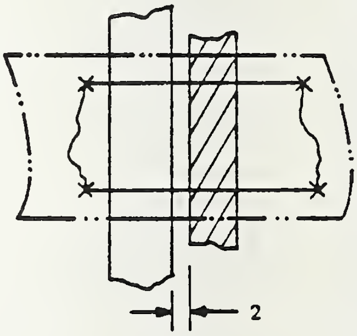
e. Level 5: Contact

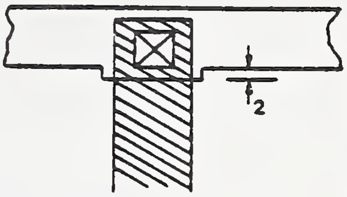
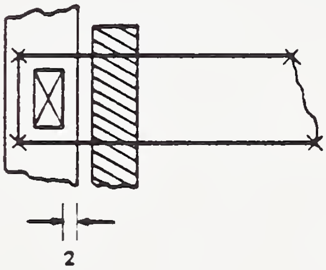
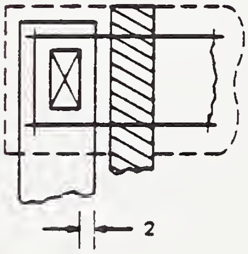
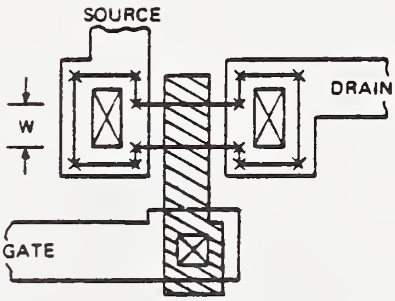
Rule #	Item	Minimum Value μm (mil)	Illustration Value (μm)
5.1	Active Contact Area	5 x 7 (0.2 x 0.28) or 6 x 6 (0.24 x 0.24)	
5.2	Contact Area in Level 5 Mask	5 x 10 (0.2 x 0.4) or 6 x 6 (0.24 x 0.24)	
5.3	Spacing, Contact to Polysilicon Gate	5 (0.2)	 
5.4	All Contacts to Polysilicon shall be Outside of n^+ Diffusion Mask.		
5.5	Contact of Polysilicon over Active Transistor is not allowed.		

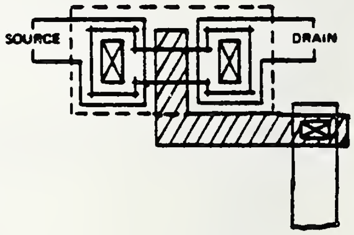
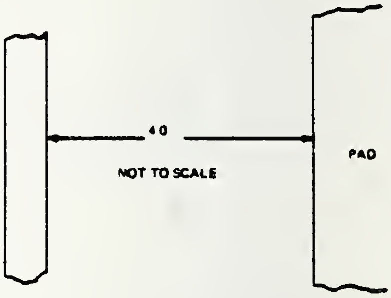
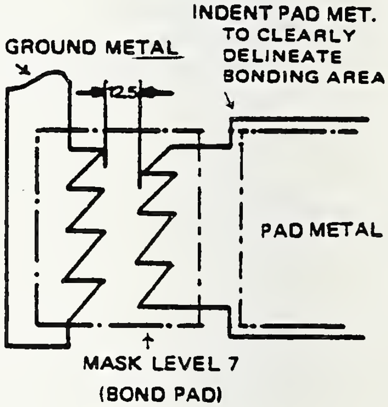
Rule #	Item	Minimum Value µm (mil)	Illustration Value (µm)
5.6	Spacing, Contact to Epi on Epi	2 (0.08) On All Sides	
5.7	Spacing, Contact to Poly on Poly	2 (0.08) On All Sides	
5.8	Overlap of Contact Over Epi Edge or Over Poly Edge onto Sapphire	Not Allowed	

f. Level 6: Metal

Rule #	Item	Minimum Value µm (mil)	Illustration Value (µm)
6.1	Width of Metal	8 (0.32)	
6.2	Spacing, Metal to Metal	6 (0.24)	
6.3.1	Spacing, Metal to NMOS Island	2 (0.08)	
6.3.2.	Spacing, Metal to PMOS Island	2 (0.08)	
NOTE	Metal should not be coincident with any edge.		

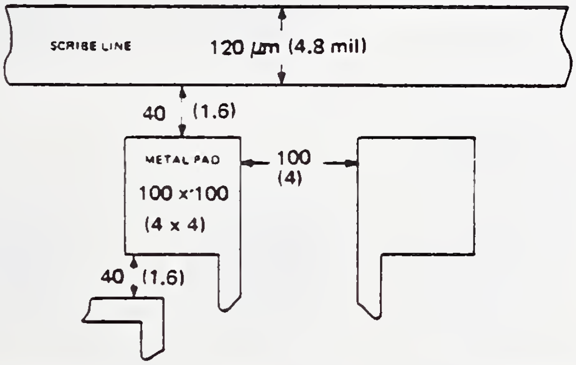
Rule #	Item	Minimum Value µm (mil)	Illustration Value (µm)
6.4	Spacing, Metal to n^+ Diffusion	0 Coincidence Is Allowed	
6.4.1	Spacing, Metal to p^+ Diffusion	0 Coincidence Is Allowed	
6.5	Metal and Polysilicon Edge Should not be Coincident		
6.6.1	Spacing, Metal to Polysilicon Gate (n-channel)	2 (0.08)	
6.6.2	Spacing, Metal to Polysilicon Gate (p-channel)	2 (0.08)	

Rule #	Item	Minimum Value μm (mil)	Illustration Value (μm)
6.7	Spacing, Metal to Contact on Poly Tunnel	2 (0.08)	
NOTE	Metal encompasses contact completely.		
6.7.1	Spacing, Metal to Contact on PMOS Island	2 (0.08)	
6.7.2	Spacing, Metal to Contact on NMOS Island	2 (0.08)	
6.7.3	p-channel Transistor when 7.5 $\mu m \le W \le 15 \mu m$		
NOTE	Metal encompasses contact completely.		

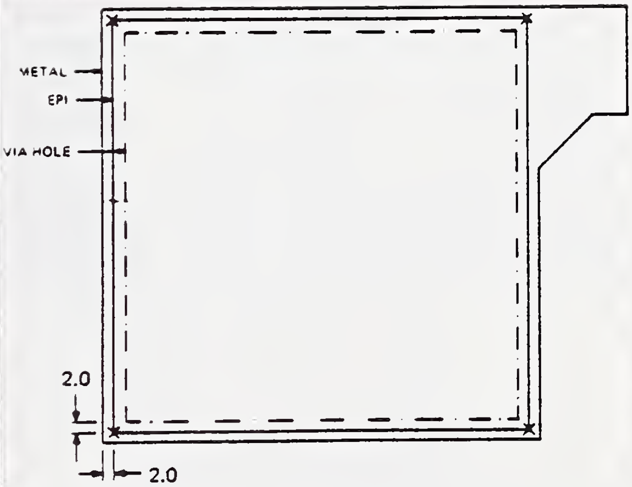
Rule #	Item	Minimum Value µm (mil)	Illustration Value (µm)
6.7.4	n-channel Device when 7.5 µm ≤ W ≤ 15 µm 0.3 mil ≤ W ≤ 0.6 mil		
NOTE	Metal encompasses contact completely.		
6.8	Spacing, Metal to Pad Metal (Except Arc Gap)	40 (1.6)	
6.9	Arc Gap between Ground Metal to Pad Metal is 12.5 µm (0.5 mil)		 INDENT PAD MET. TO CLEARLY DELINEATE BONDING AREA GROUND METAL 12.5 PAD METAL MASK LEVEL 7 (BOND PAD)
6.10	Overlap, Pad Metal to PMOS Island is 2 µm (0.08 mil)		See Illustration on Rule # 7.1

Rule #	Item	Minimum Value µm (mil)	Illustration Value (µm)
6.11	Pad Size	100 x 100 (4.0 x 4.0)	
6.11.1	Spacing, Pad to Pad	100 (4.0)	
6.11.1	Spacing, Pad to Metal Line	40 (1.6)	
6.12	Width of Scribe Line	120 (4.8)	
6.12	Spacing, Scribe Line to Pad	40 (1.6)	

Metal Pad and Scribe Line



g. Level 7: Bond Pad

Rule #	Item	Illustration Value (µm)
7.1	Epi Overlap to Via Hole is 2.0 µm (0.08 mil)	

Appendix B

NBS-16 AND NBS-26 TEST STRUCTURE DESCRIPTION

Introduction

This appendix describes the structures designed by NBS and included on the test patterns NBS-16 and NBS-26. NBS-16 is illustrated in figure B-1.

This appendix contains a number of figures produced on a computer-controlled plotter. Figure B-2 is a key for identifying the individual levels. Many structures require a change in only the level position of the implant mask to form a new device (e.g., *p*-channel *versus* *n*-channel MOSFET). Only one figure has been included in this report for each basic structure. Similar structures, varying only in the level of the implant mask, are grouped in this listing. The figures show, in each case, the levels associated with the first structure of the group.

A description of the method used to measure the MOSFET electrical parameters is found elsewhere [B-1].

I. Process Parameter Pattern

Purpose: The process parameter portion contains structures necessary to evaluate baseline electrical parameters.

Description: The process parameter patterns on test patterns NBS-16 and NBS-26 are laid out in 2 by N columns of probe pads. The pattern is a square approximately 100 mil (2.54 mm) on a side. Six columns containing 28 structures are present. The pattern can be probed automatically by a 2 by 10 probe card and computer tester. Structures 1 through 28 appear on NBS-16. The process parameter pattern on test pattern NBS-26 is laid out similarly to NBS-16 and contains 35 structures. Test structures 1 through 26 and 38 through 46 appear on NBS-26.

Drawings: NBS-16, figure B-3; NBS-26, figure B-4. (The structure numbers appear in the upper left probe pad of each structure.)

List of Structures

1. *p*-channel four-terminal MOSFET
2. *n*-channel four-terminal MOSFET
   a. Description: This device is a conventional MOSFET with electrical contacts to gate, source, drain, and body. The gate dimensions are 2.5 by 0.3 mil (0.064 by 0.0076 mm).
   b. Parameters determined: Threshold voltage at 1.0 μA, source-to-drain breakdown voltage at 10.0 μA, source-to-drain leakage current at 10.0 V, calculated conduction factor k', calculated threshold voltage, and the standard error of estimate of the two calculated parameters.
   c. Drawing: Figure B-5.
3. *p*-channel five-terminal MOSFET

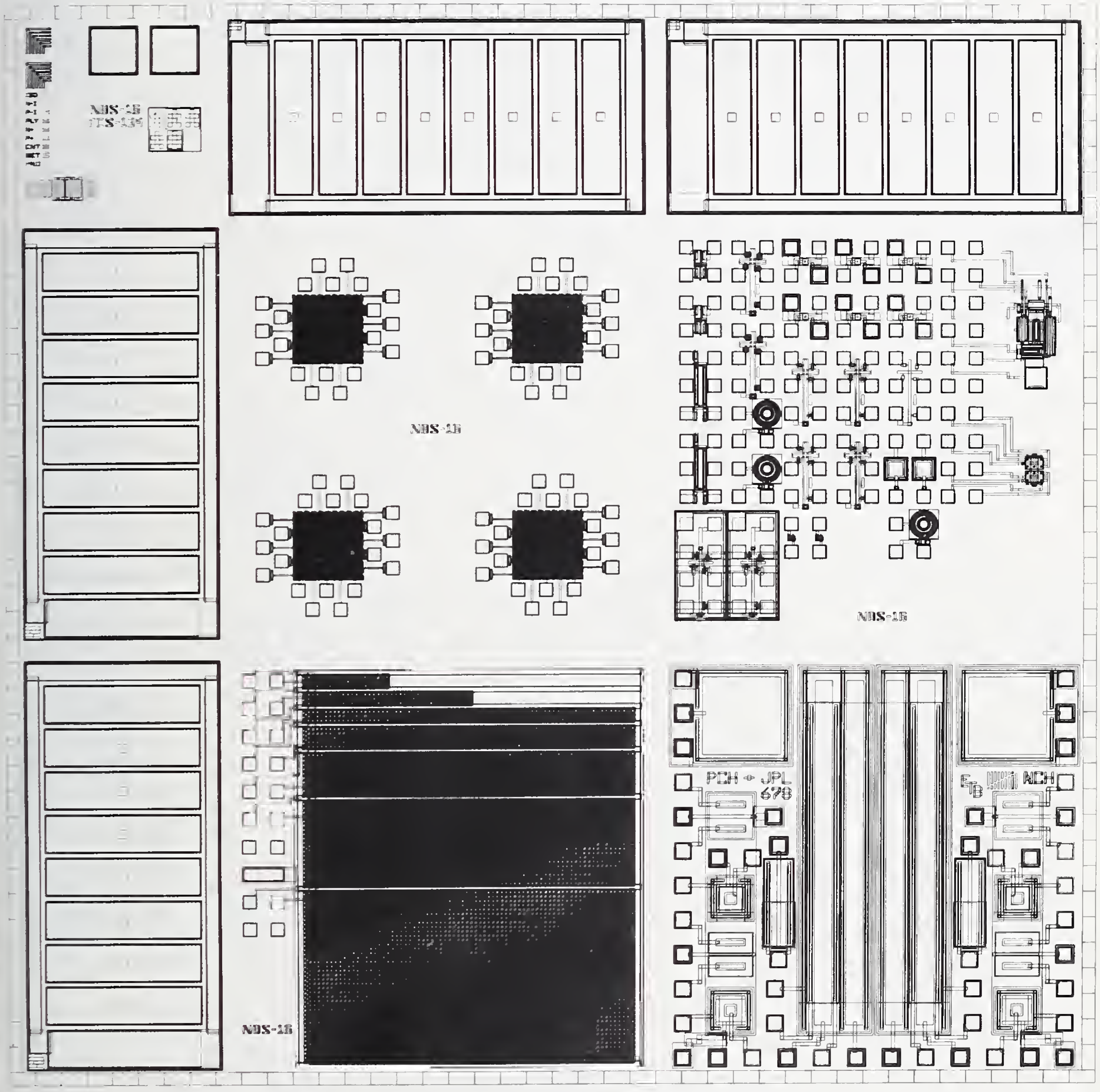


Figure B-1. NBS-16 test pattern.

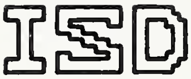
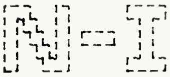
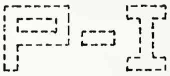
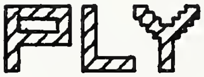
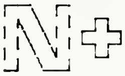
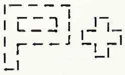
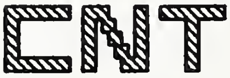
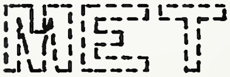
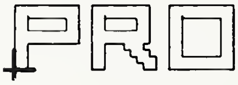
	Process Sequence	Function
 ISD	1.	Island Definition
 N-I	2.	N- Implant
 P-I	3.	P- Implant
 PLY	4.	Poly Definition
 N+	5.	N+ Implant
 P+	6.	P+ Implant
 CNT	7.	Contact
 MET	8.	Metal Definition
 PRO	9.	Passivation

Figure B-2. Level identification key.

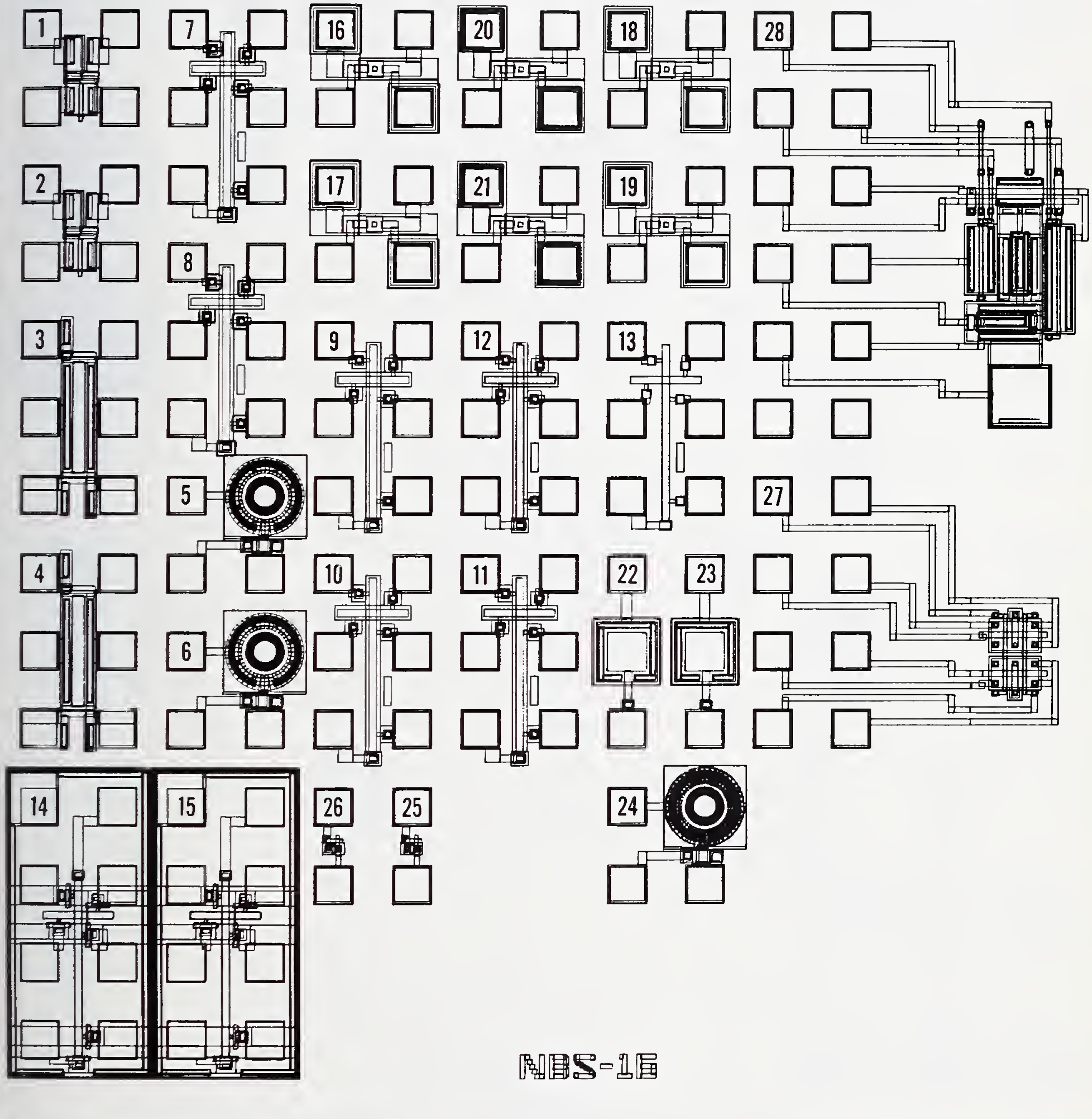


Figure B-3. Process parameter pattern, test pattern NBS-16.

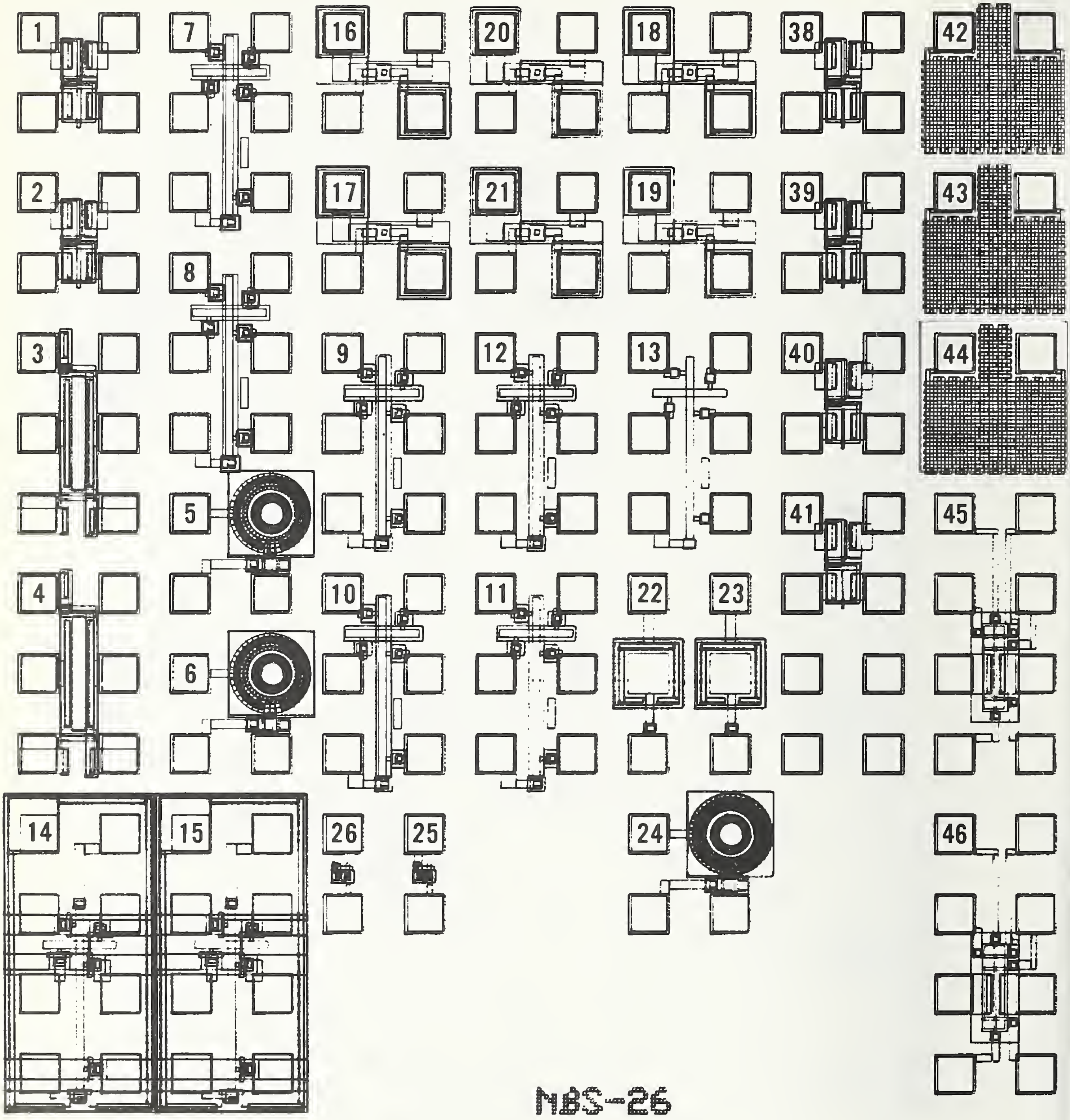


Figure B-4. Process parameter pattern, test pattern NBS-26.

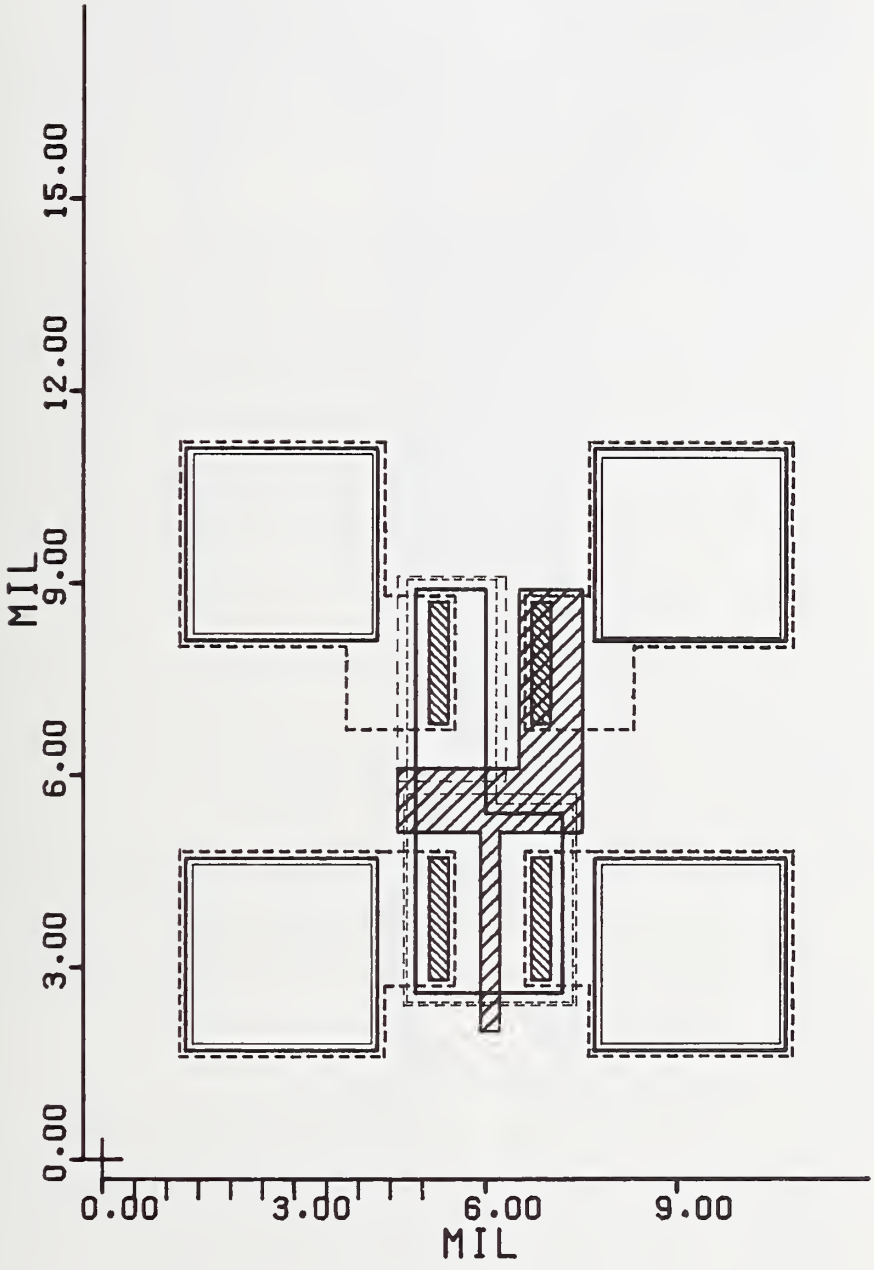


Figure B-5. Four-terminal MOSFET.

4. *n*-channel five-terminal MOSFET
   - a. Description: This device is a five-terminal MOSFET with electrical contacts to gate, source, and drain, and two contacts to the body. The device is much larger than Devices 1 and 2, but it has approximately the same length-to-width ratio. The gate dimensions are 9.0 by 1.0 mil (2.3 by 0.025 mm).
   - b. Parameters determined: Threshold voltage at 1.0 μA, source-to-drain breakdown voltage at 10.0 μA, source-to-drain leakage current at 10.0 V, calculated conduction factor k', calculated threshold voltage, and the standard error of estimate of the two calculated parameters.
   - c. Drawing: Figure B-6.
5. *n*-channel closed geometry MOSFET
6. *p*-channel closed geometry MOSFET
   - a. Description: This device is a four-terminal MOSFET with electrical connection to gate, source, drain, and body. It is a circular device with the source completely surrounded by the gate channel and the gate channel surrounded by the drain. The gate channel is "edgeless"; it has a length of 0.3 mil (0.0076 mm).
   - b. Parameters determined: Threshold voltage at 1.0 μA, source-to-drain breakdown voltage at 10.0 μA, source-to-drain leakage current at 10.0 V, calculated conduction factor k', calculated threshold voltage, and the standard error of estimate of the two calculated parameters.
   - c. Drawing: Figure B-7.
7. p^- cross-bridge sheet resistor
8. n^- cross-bridge sheet resistor
9. p^+ cross-bridge sheet resistor
10. n^+ cross-bridge sheet resistor
11. p^+ doped poly cross-bridge sheet resistor
12. n^+ doped poly cross-bridge sheet resistor
13. Metal cross-bridge sheet resistor
    - a. Description: The cross-bridge sheet resistor is a combination of a van der Pauw sheet resistor and a bridge resistor [B-2]. The design linewidth is 0.6 mil (0.015 mm).
    - b. Parameters measured: Sheet resistance and linewidth of the conducting layer.
    - c. Drawing: Figure B-8.
14. p^- gated cross-bridge sheet resistor
15. n^- gated cross-bridge sheet resistor
    - a. Description: The gated cross-bridge sheet resistor is similar in geometry to Device no. 7 except that the resistor is junction isolated in an epi island. The resistor is defined by a polysilicon gate which is a mask for a further heavy channel stop implant. Electrical contact is made to the resistor (or channel region), the poly gate, and the channel stop.
    - b. Parameters measured: Sheet resistance and linewidth of the channel region with the gate grounded.
    - c. Drawing: Figure B-9.
16. Metal to p^- contact resistor
17. Metal to n^- contact resistor
18. Metal to p^+ contact resistor
19. Metal to n^+ contact resistor

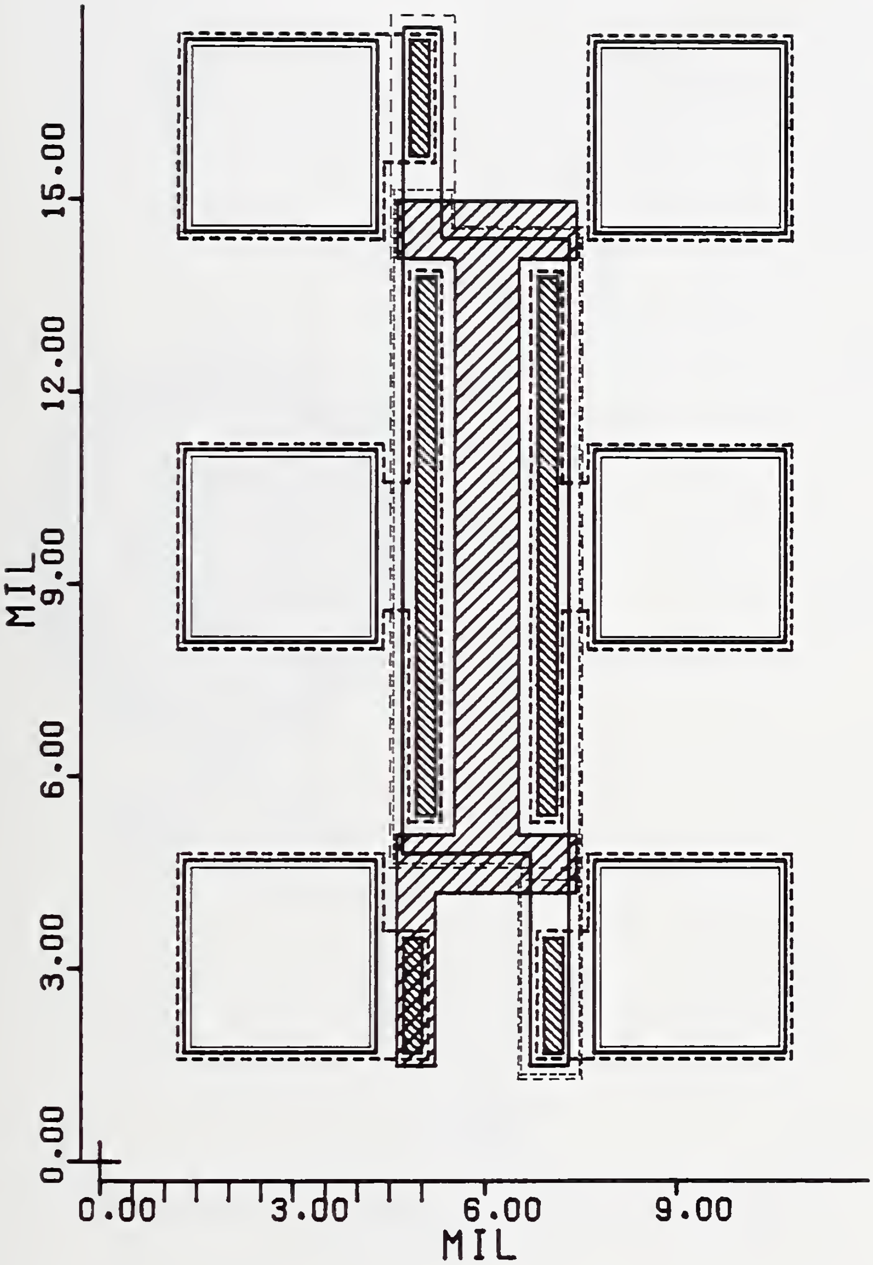


Figure B-6. Five-terminal MOSFET.

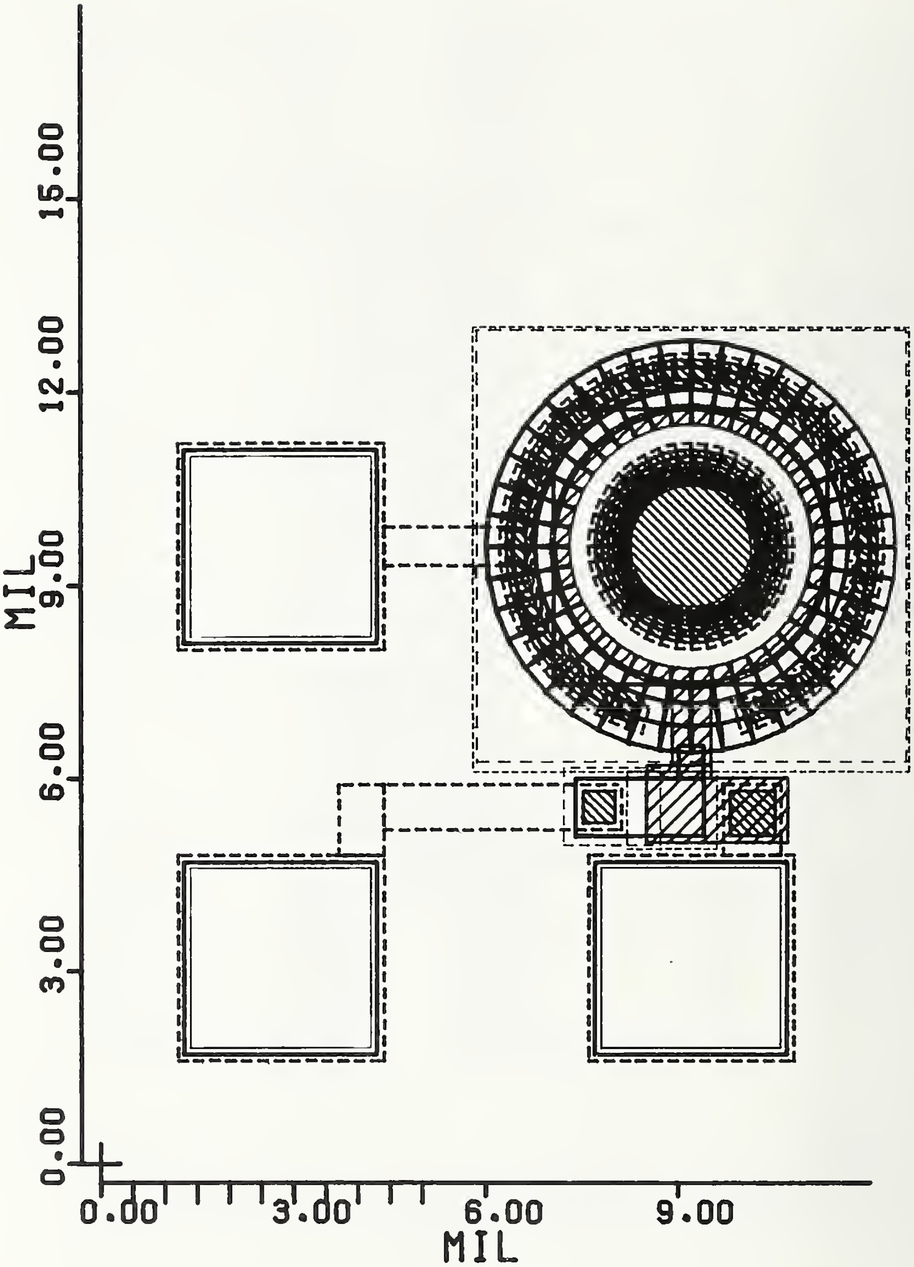


Figure B-7. Closed geometry MOSFET.

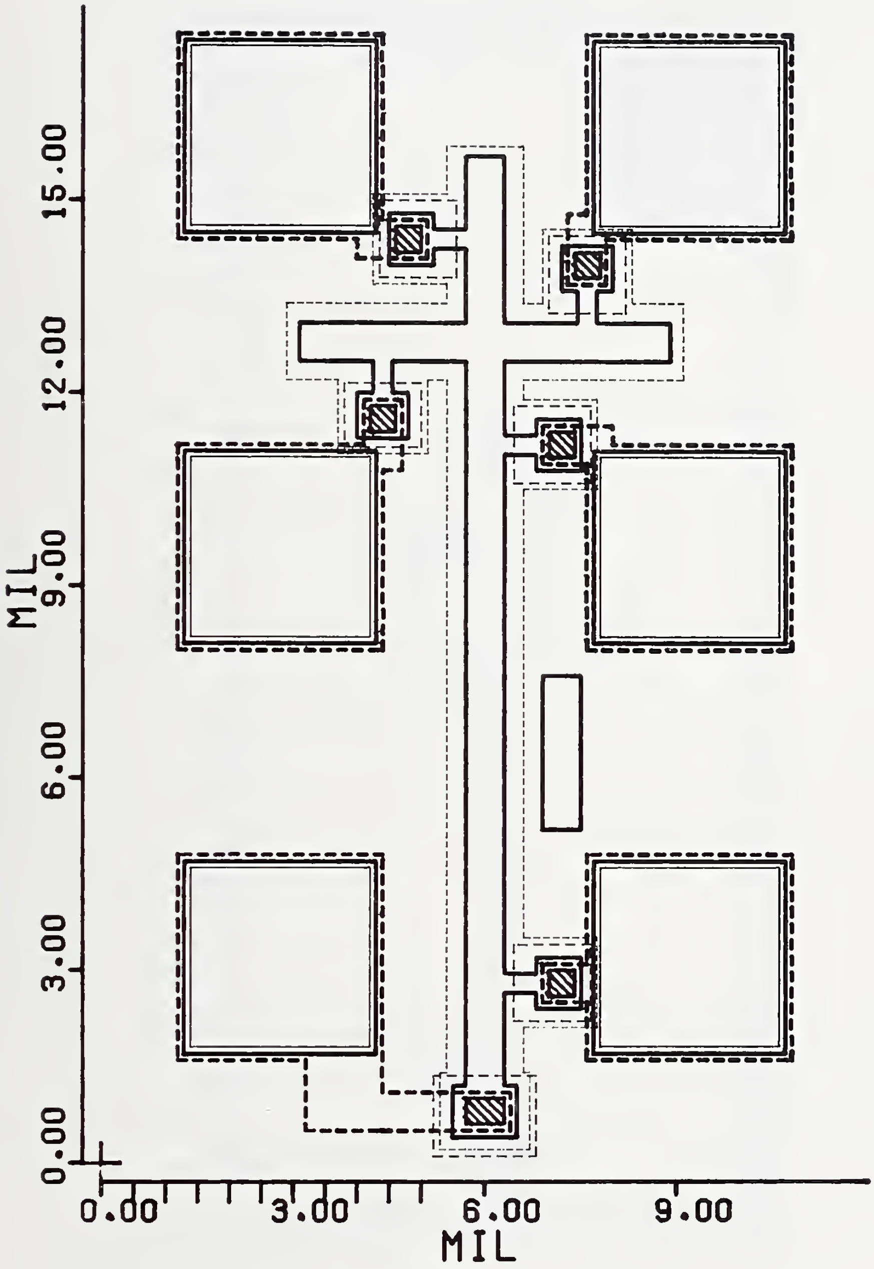


Figure B-8. Cross-bridge sheet resistor.

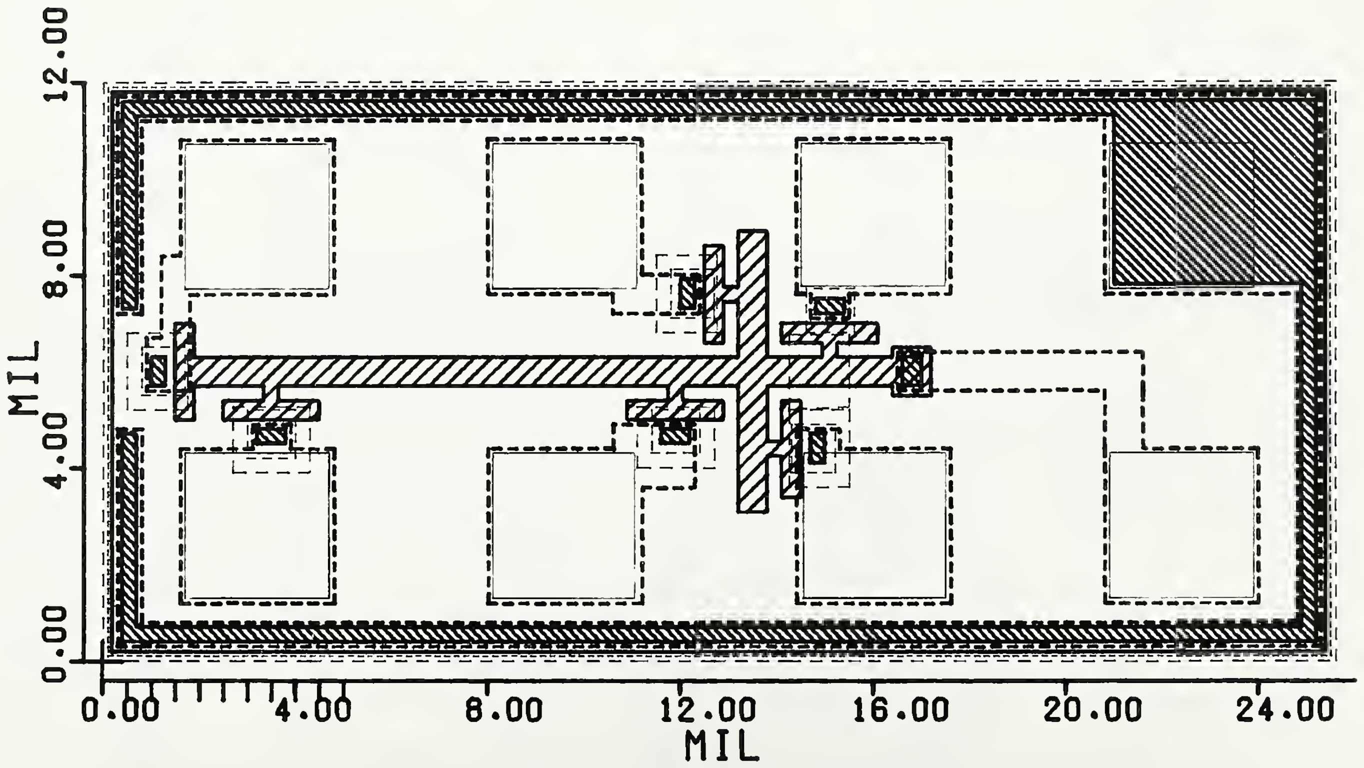


Figure B-9. Gated cross-bridge sheet resistor.

20. Metal to p^+ doped poly contact resistor
21. Metal to n^+ doped poly contact resistor
    a. Description: The contact resistor is used to measure the electrical resistance between the metal level and a resistive layer [B-3]. The size of the contact opening is a square 0.4 mil (0.010 mm) on a side. This is the same size contact opening used on the cross-bridge sheet resistor.
    b. Parameters measured: Contact resistance.
    c. Drawing: Figure B-10.
23. *n*-type MOS capacitor
    a. Description: This structure is a poly-oxide-epi capacitor with an area of 10.24 mil^2 (6.61×10^{-3} mm^2) and with an electrical guard ring.
    b. Parameters measured: Capacitance per unit area and possibly capacitance *versus* voltage characteristics.
    c. Drawing: Figure B-11.
24. Closed geometry gated diode
    a. Description: This device is similar to the closed geometry MOSFET (Device no. 5) except that the gate is extended beyond the drain region and off the epi island. The electrical connection to the drain has been removed, leaving electrical connection to the source, body, and gate.
    b. Parameters measured: Leakage current caused by bulk and surface carrier generation.
    c. Drawing: Figure B-12.
25. *n*-channel two-terminal MOSFET
26. *p*-channel two-terminal MOSFET
    a. Description: This structure is a two-terminal MOSFET with the gate permanently connected to the drain. It is used as the internal cell in the Random Fault Structure I MOSFET arrays. It is included here to permit electrical access to a single cell.
    b. Parameters measured: Threshold voltage at 1.0 μA, source-to-drain breakdown voltage at 10.0 μA, and source-to-drain leakage current at 10.0 V.
    c. Drawing: Figure B-13.
27. Internal cell from RCA Gate Universal Array (GUA)
    a. Description: This is an internal cell from the RCA GUA family and has been included to provide electrical access to an individual structure used frequently in the RCA GUAs. The cell consists of two *p*-channel and two *n*-channel MOSFETs [B-4].
    b. Parameters determined: Threshold voltage at 1.0 μA, source-to-drain breakdown voltage at 10.0 μA, source-to-drain leakage current at 10.0 V, calculated conduction factor k', calculated threshold voltage, and the standard error of estimate of the two calculated parameters.
    c. Drawing: Figure B-14.
28. Input/Output cell with input protection from RCA GUA
    a. Description: This is an input/output cell consisting of a *p*-channel and *n*-channel MOSFET, two diodes, and a resistor [B-4]. The diodes and resistor are arranged so they can be included in input structures or omitted in output structures. The device on NBS-16 has no components internally connected. Each device is connected to a probe pad for electrical access.

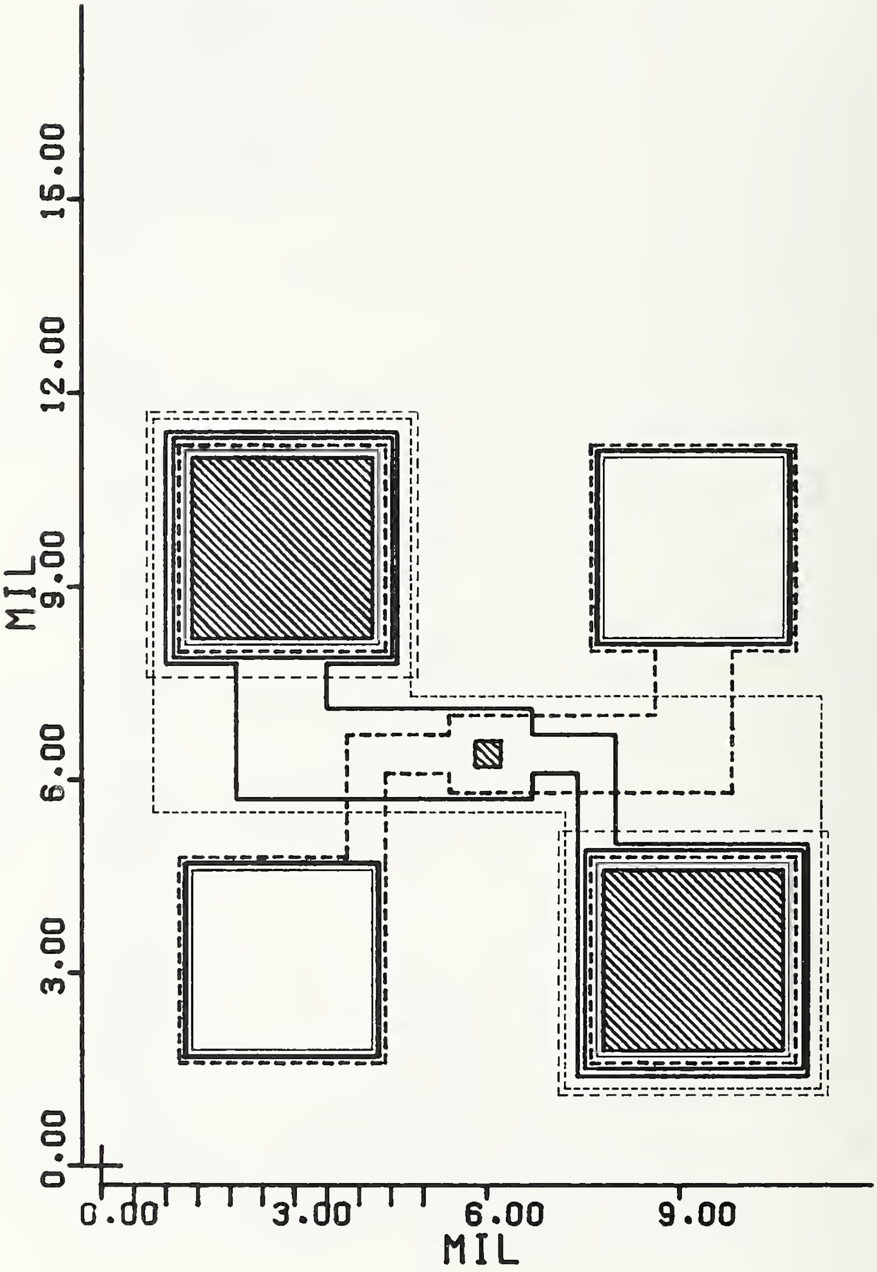


Figure B-10. Contact resistor.

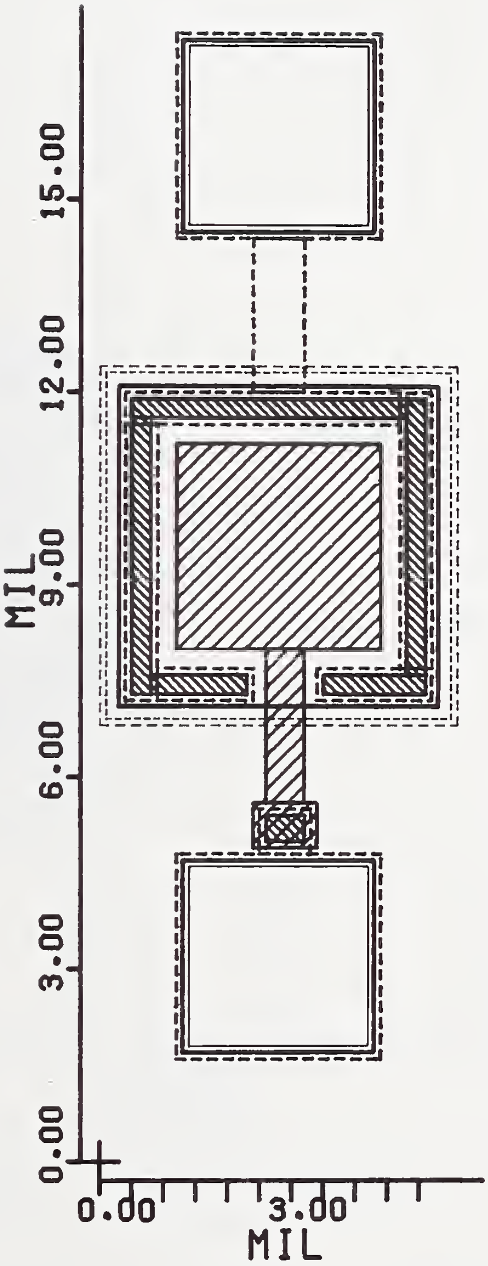


Figure B-11. MOS capacitor.

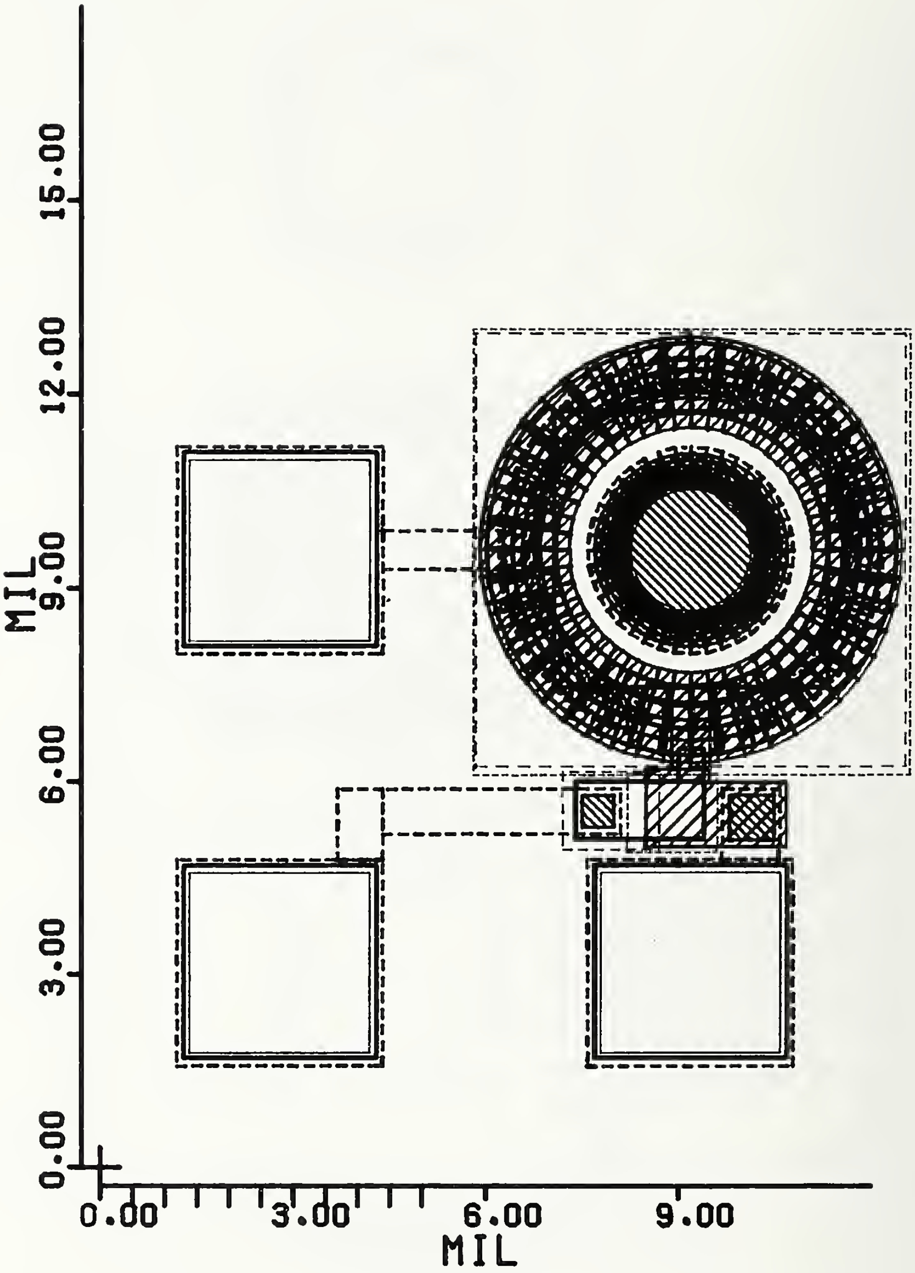


Figure B-12. Closed geometry gated diode,

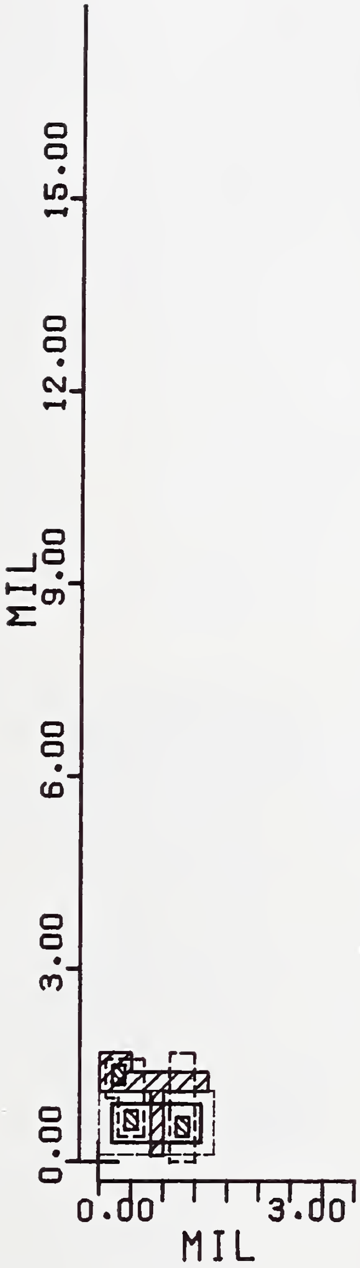


Figure B-13. Two-terminal MOSFET.

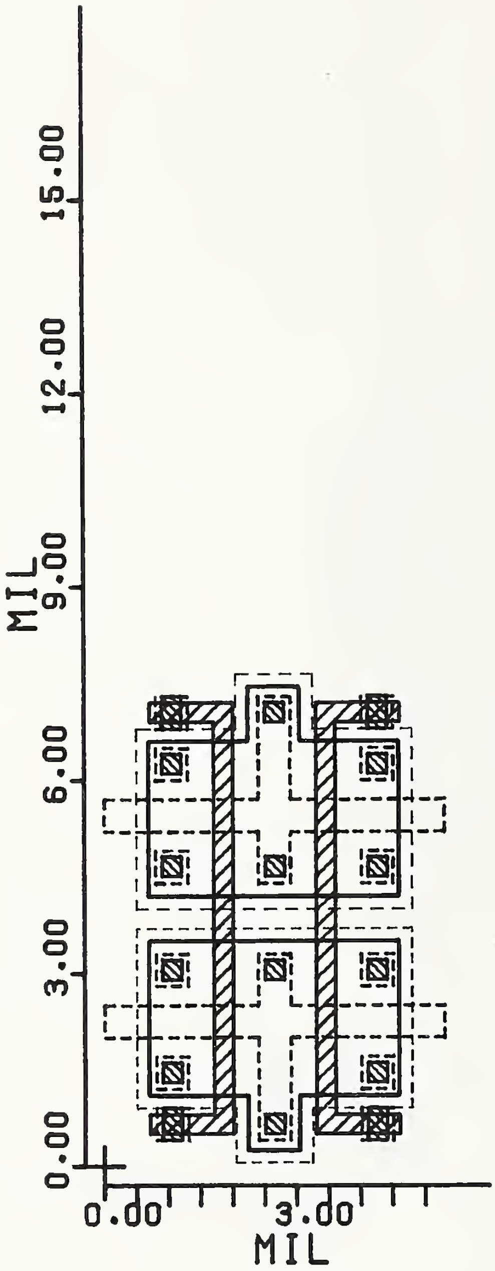


Figure B-14. Internal cell from RCA Gate Universal Array.

   b. Parameters determined: Threshold voltage at 1.0 μA, source-to-drain breakdown voltage at 10.0 μA, source-to-drain leakage current at 10.0 V, calculated conduction factor k', calculated threshold voltage, and the standard error of estimate of the two calculated parameters. *pn* junction characteristics.
   c. Drawing: Figure B-15.

38. *p*-channel four-terminal MOSFET
39. *n*-channel four-terminal MOSFET
   a. Description: This device is a conventional MOSFET with electrical contacts to gate, source, drain, and body. The gate dimensions are 2.5 by 0.2 mil (0.064 by 0.0051 mm).
   b. Parameters determined: Threshold voltage at 1.0 μA, source-to-drain breakdown voltage at 10.0 μA, source-to-drain leakage current at 10.0 V, calculated conduction factor k', calculated threshold voltage, and the standard error of estimate of the two calculated parameters.
   c. Drawing: Figure B-5.
40. *p*-channel four-terminal MOSFET
41. *n*-channel four-terminal MOSFET
   a. Description: This device is a conventional MOSFET with electrical contacts to gate, source, drain, and body. The gate dimensions are 2.5 by 0.15 mil (0.064 by 0.0038 mm).
   b. Parameters determined: Threshold voltage at 1.0 μA, source-to-drain breakdown voltage at 10.0 μA, source-to-drain leakage current at 10.0 V, calculated conduction factor k', calculated threshold voltage, and the standard error of estimate of the two calculated parameters.
   c. Drawing: Figure B-5.
42. Metal-over-island step coverage structure
   a. Description: This structure is a two-terminal resistor designed to evaluate metal-over-island electrical continuity. The structure consists of a 0.3-mil (0.0076-mm) serpentine metallization line crossing a parallel array of 0.3-mil (0.0076-mm) epi islands at 488 steps.
   b. Parameters determined: Electrical continuity and resistance.
   c. Drawing: Figure B-16.
43. Metal-over-poly step coverage structure
   a. Description: This structure is a two-terminal resistor design to evaluate metal-over-poly electrical continuity. The structure consists of a 0.3-mil (0.0076-mm) serpentine metallization line crossing a parallel array of 0.3-mil (0.0076-mm) poly lines at 488 steps.
   b. Parameters determined: Electrical continuity and resistance.
   c. Drawing: Figure B-17.
44. Metal-over-poly on island step coverage structure
   a. Description: This structure is a two-terminal resistor designed to evaluate the electrical continuity of metal-over-poly when the poly is over an epi island. The structure consists of a 0.3-mil (0.0076-mm) serpentine metallization line crossing a parallel array of 0.3-mil (0.0076-mm) poly lines at 488 steps.
   b. Parameters determined: Electrical continuity and resistance.
   c. Drawing: Figure B-18.
45. *p*-channel MOSFET cross-bridge sheet resistor

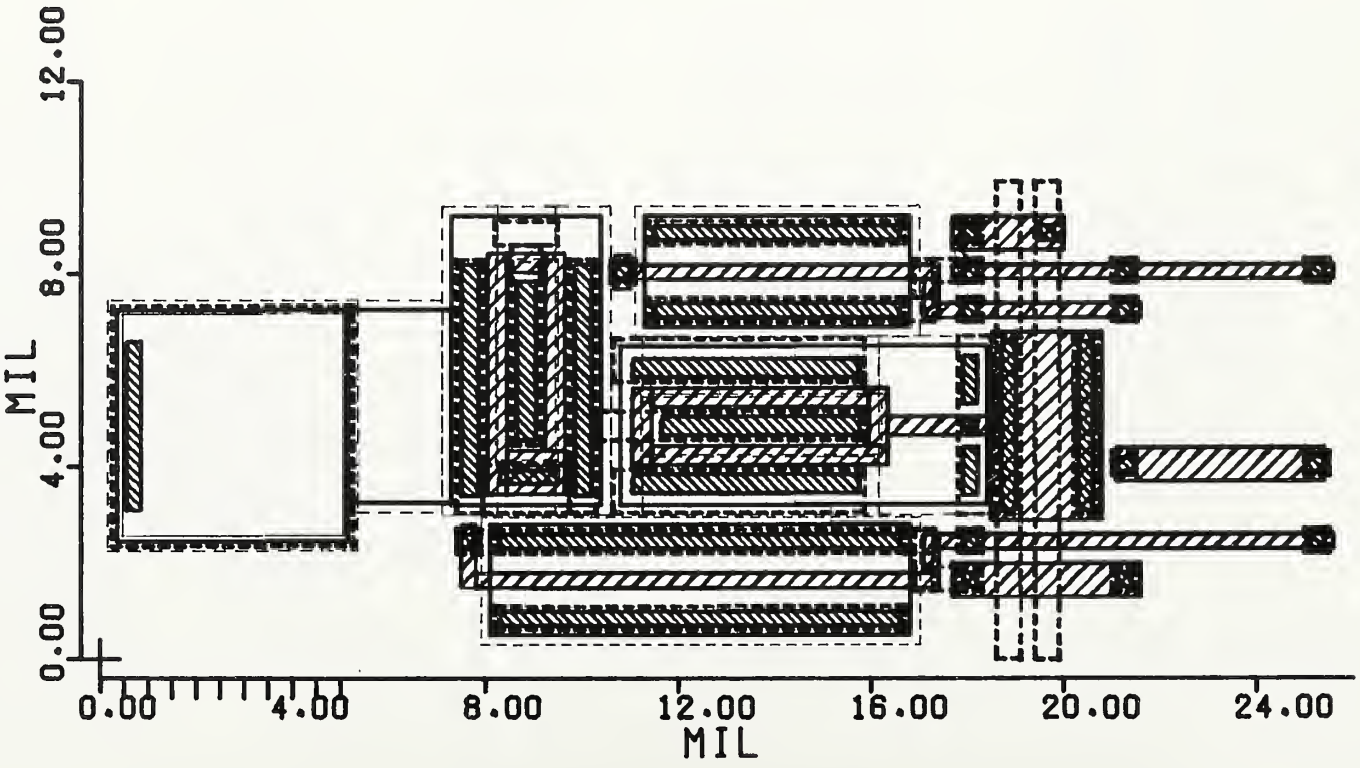


Figure B-15. Input/output cell with input protection from RCA GUA.

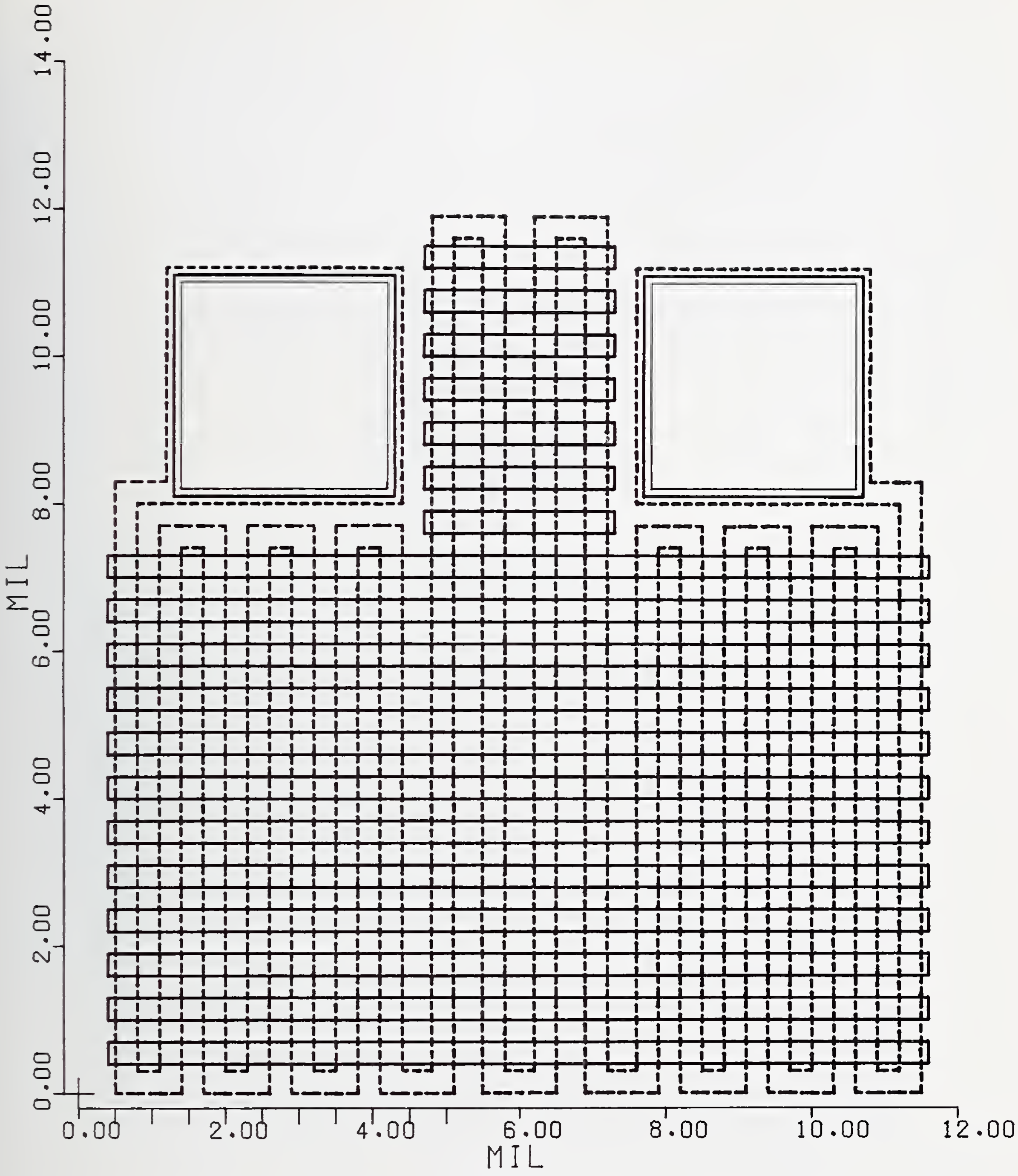


Figure B-16. Metal-over-island step coverage structure.

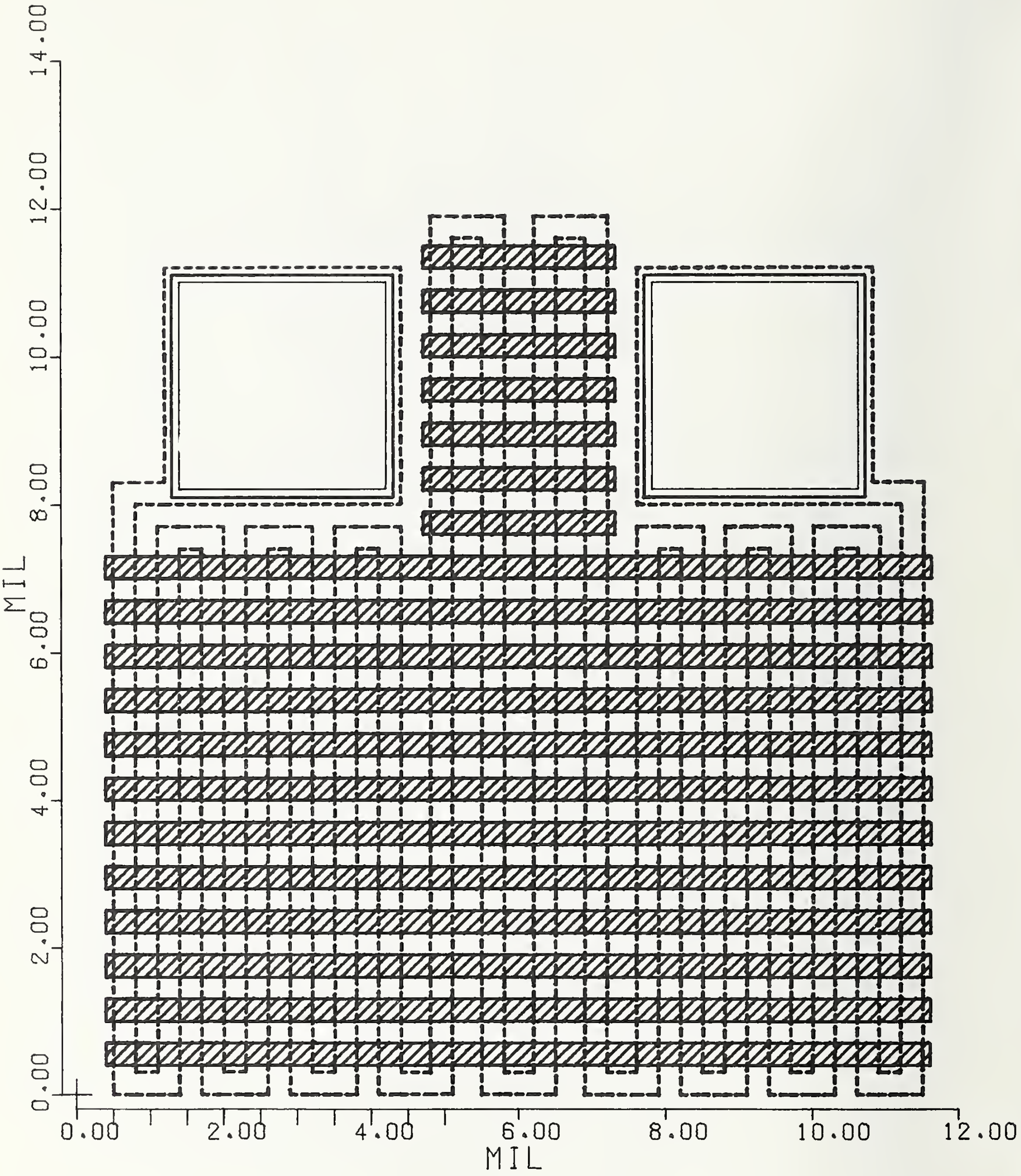


Figure B-17. Metal-over-poly step coverage structure.

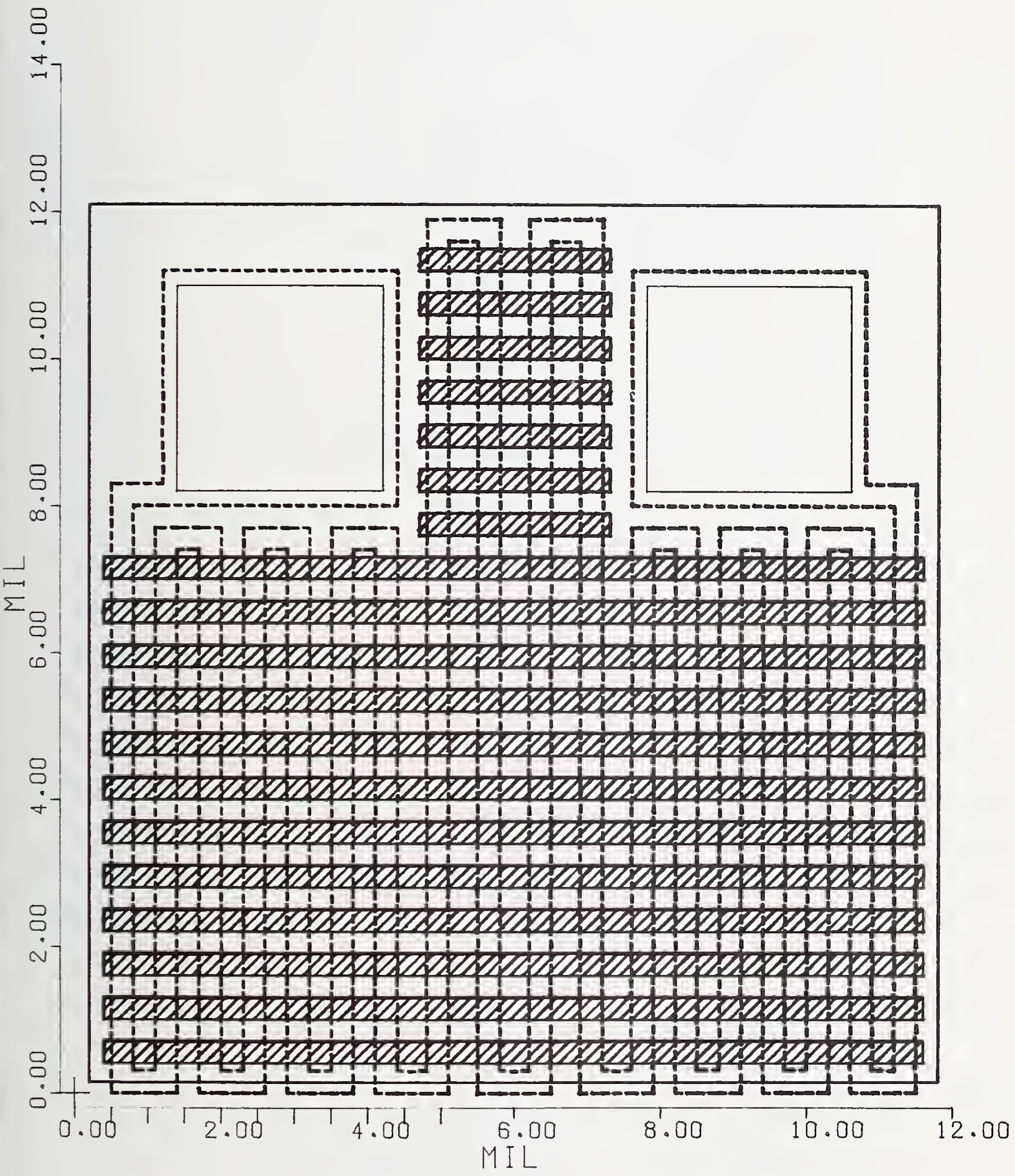


Figure B-18. Metal-over-poly on island step coverage structure.

46. *n*-channel MOSFET cross-bridge sheet resistor
    a. Description: This is a developmental test structure which consists of a three-terminal MOSFET with a polysilicon cross-bridge sheet resistor as the gate electrode. The structure may be useful in determining correlations between MOSFET electrical parameter variations and changes in the linewidth and sheet resistance of the gate.
    b. Parameters determined: Threshold voltage at 1.0 μA, source-to-drain breakdown voltage at 10.0 μA, source-to-drain leakage current at 10.0 V, calculated conduction factor k', calculated threshold voltage, the standard error of estimate of the two calculated parameters, and sheet resistance and linewidth of the gate electrode.
    c. Drawing: Figure B-19.

II. Physical Analysis Pattern

Purpose: The physical analysis portion of NBS-16 contains structures which are intended for physical, visual, or beam analysis. No electrical testing is performed with these structures.

Description: The physical analysis pattern is a square approximately 50 mil (1.27 mm) on a side located in the upper left corner of NBS-16. Mask alignment marks and level designators are also included in this pattern.

Drawing: Figure B-20. (The structure number appears to the left of each structure.)

List of Test Structures

29. Light-field RCA alignment marks (fig. B-21)
30. Dark-field RCA alignment marks (fig. B-22)
31. Mark level designators and critical dimension structures
    a. Description: This structure contains mask level designators and critical dimension structures on each level. The critical dimension structure consists of a pair of minimum width 2.0-mil (0.051-mm) long parallel lines separated by the width of one line.
    b. Parameters measured: Linewidth of critical dimensions on the working photomasks.
    c. Drawing: Figure B-23.
32. Overetch structure
    a. Description: This structure contains checkerboard elements which can be inspected visually to determine overetching or underetching for epi definition, poly-over-epi definition, metal-over-epi definition, contact-window-over-epi definition, and contact-window-over-poly definition.
    b. Parameters measured: The degree of overetching or underetching of critical levels.
    c. Drawing: Figure B-24.
33. p^- SIMS area
34. n^- SIMS area

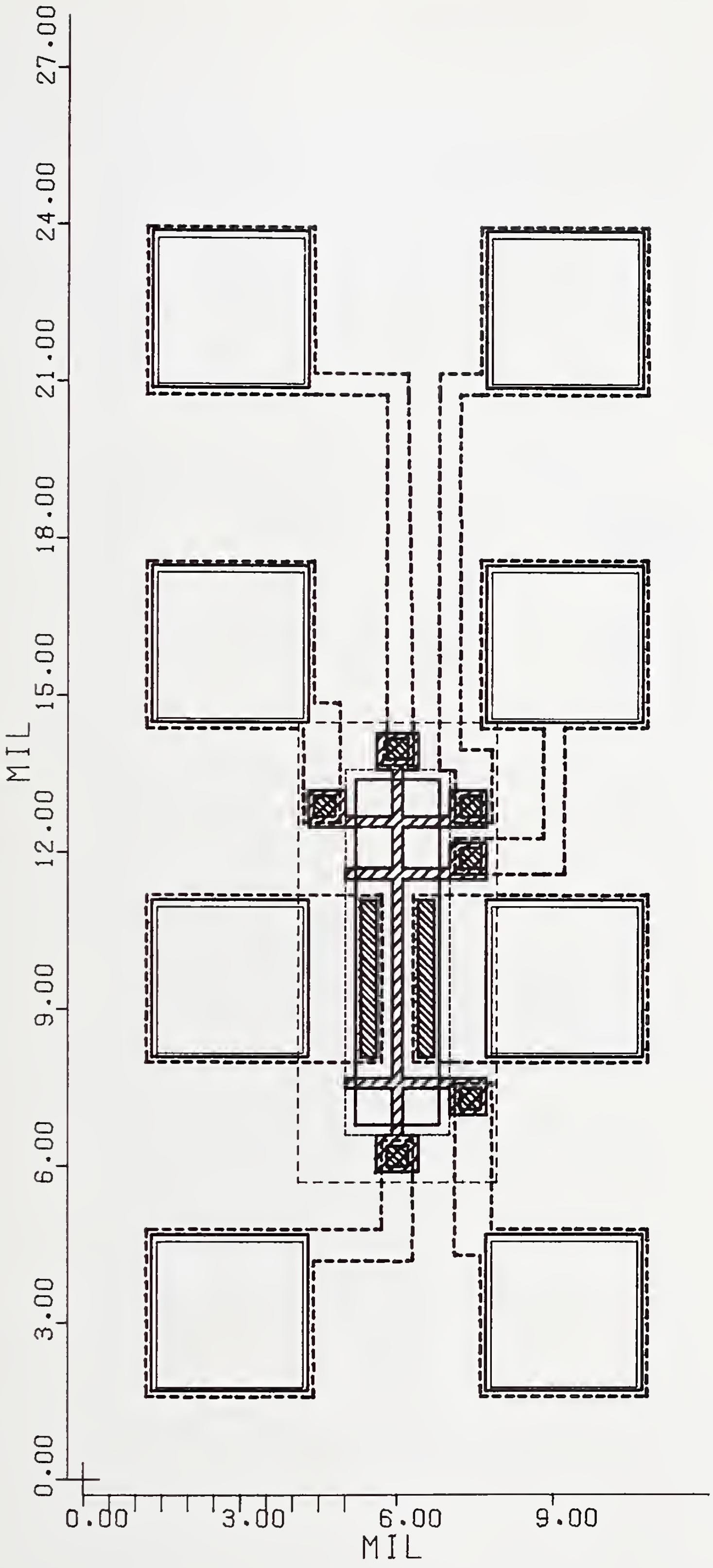


Figure B-19. MOSFET cross-bridge sheet resistor.

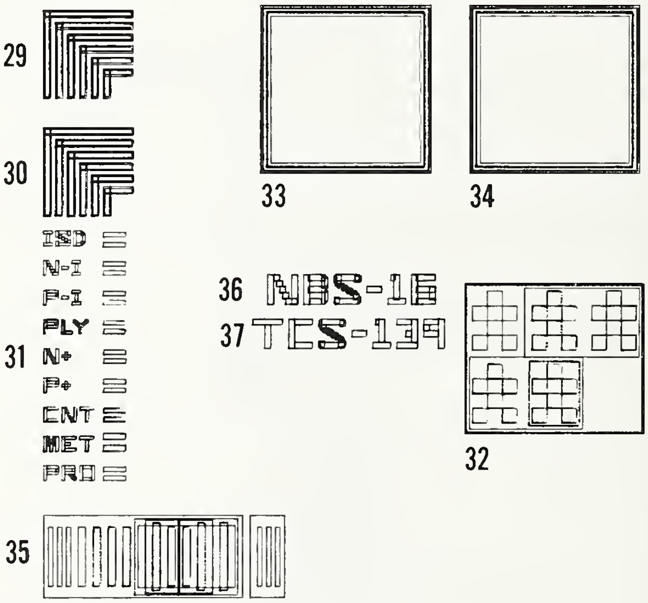


Figure B-20. NBS-16 physical analysis pattern.

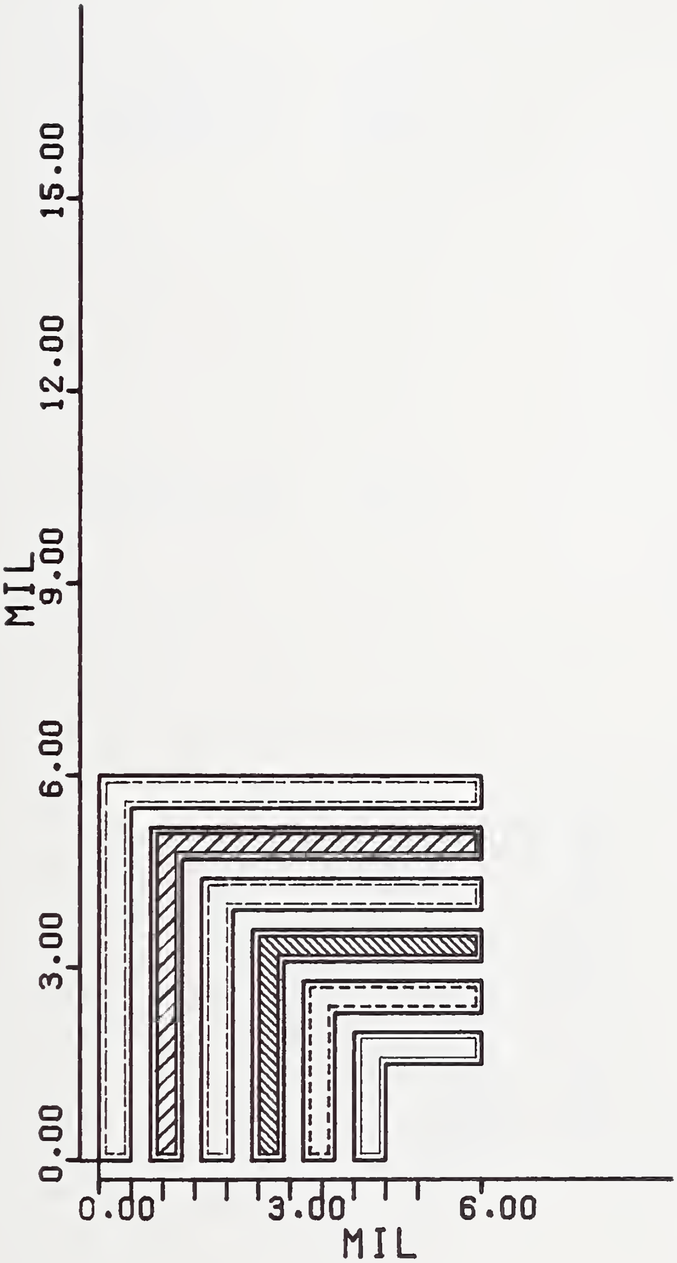


Figure B-21. Light-field RCA alignment marks.

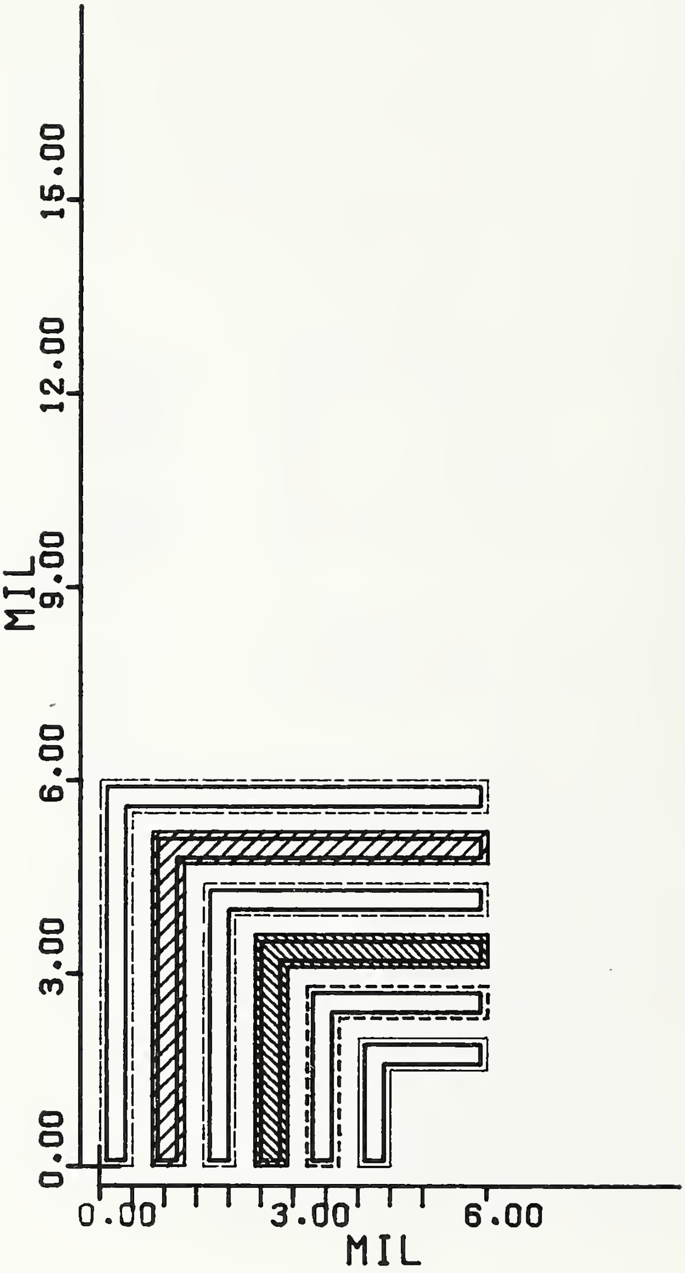


Figure B-22. Dark-field RCA alignment marks.

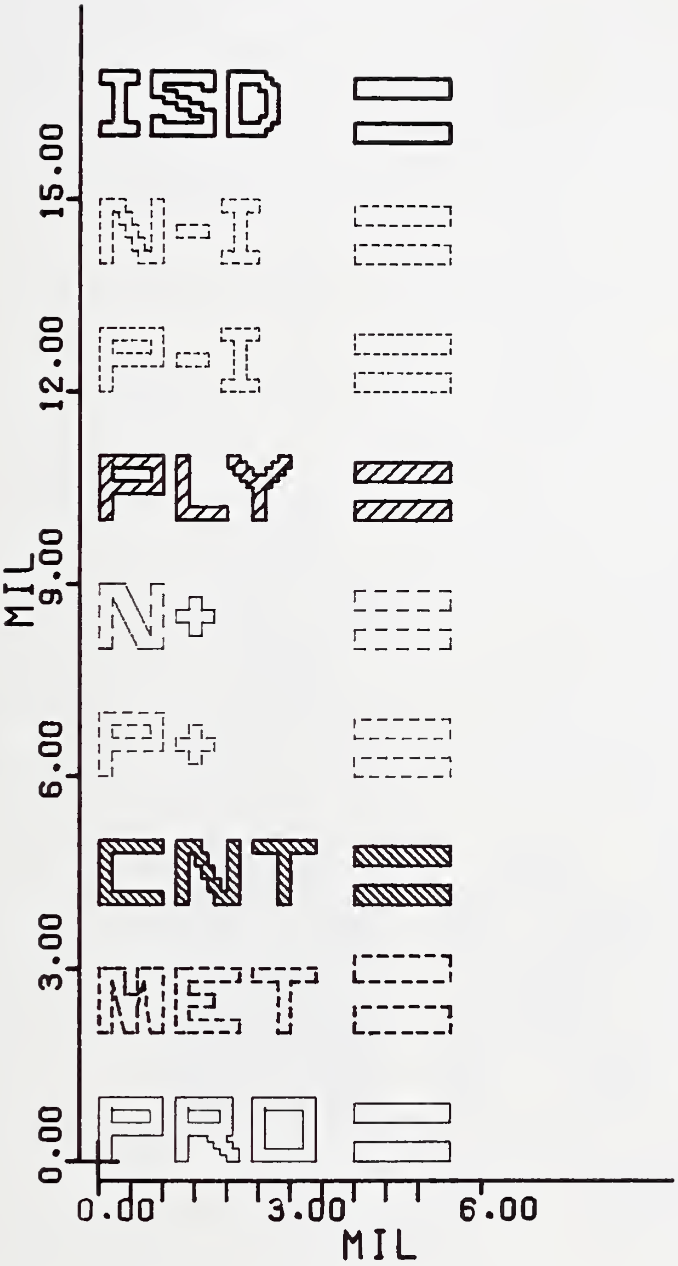


Figure B-23. Mask level designators and critical dimension structures.

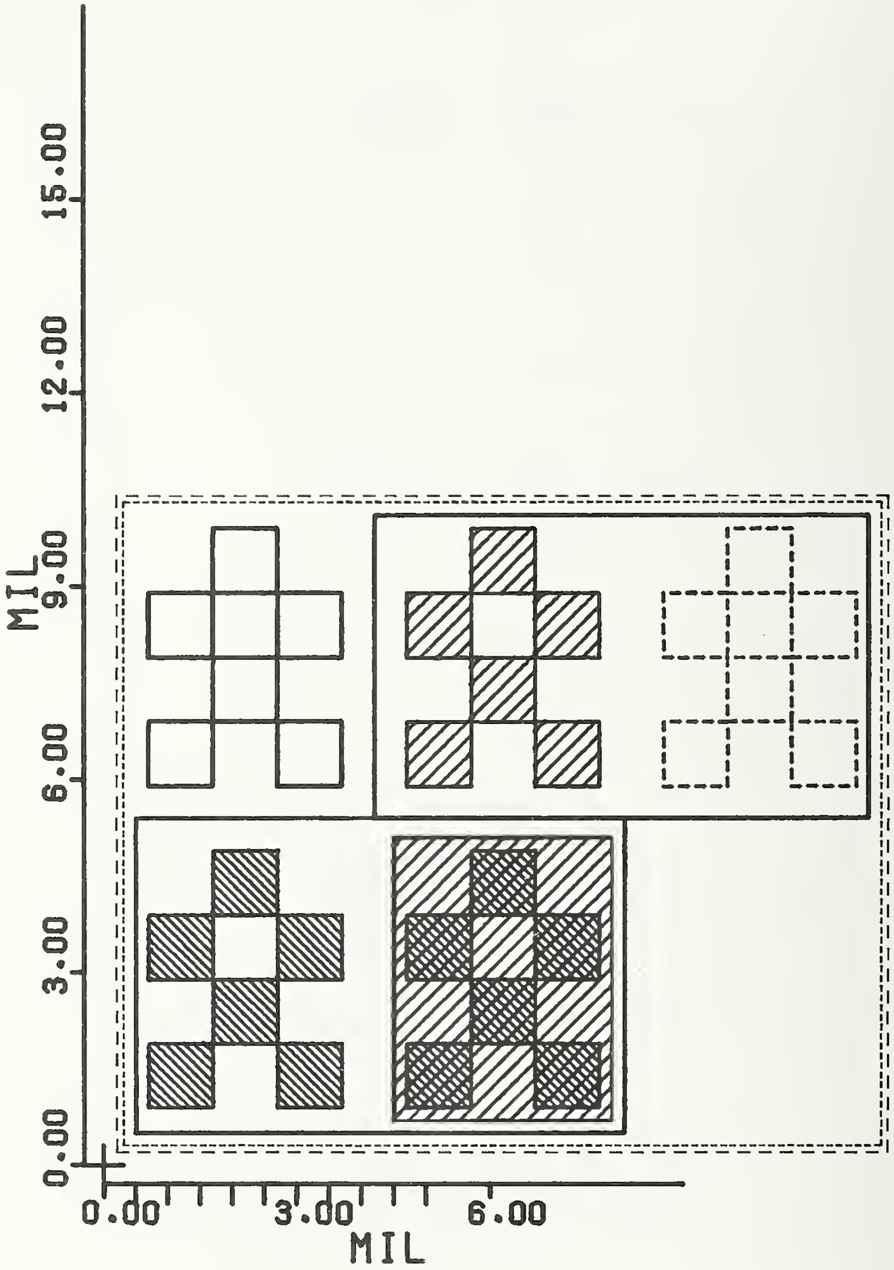


Figure B-24. Overetch structure.

a. Description: This structure is a square 10.0 mil (0.0254 mm) on a side which can be analyzed by secondary ion mass spectroscopy.
b. Parameters measured: Impurity atom concentration.
c. Drawing: Figure B-25.

35. Surface profilometer
   a. Description: This structure is a series of parallel 4.0-mil (0.10-mm) long stripes of metal, oxide, epi, and poly and is intended for use with a surface-profile-type instrument.
   b. Parameters measured: The step height of epi, poly, metal, and contact window on sapphire and the step height of poly, contact window, and metal on epi.
   c. Drawing: Figure B-26.

III. Random Access Fault Structure (RFI) - NBS-16 and NBS-26

Purpose: The purpose of this structure is to test the feasibility of using a logic type array to determine the random fault density of a MOSFET array and determine the location and nature of any faults detected. The spatial integrity of important parameters will also be determined.

Description: This structure consists of two 10 by 10 arrays of *p*-channel MOSFETs and two 10 by 10 arrays of *n*-channel MOSFETs. The arrays are within a 100-mil (2.54-mm) square. The devices are interconnected such that the drains and gates are common. They are arranged in rows and columns similar to a diode matrix with source connections to columns and the gate and drain connections to rows. Each device is electrically isolated from its neighbor and can be individually tested by addressing the appropriate row and column probe pads.

Parameters Measured: For each MOSFET in the array, threshold voltage at 1.0 μA, source-to-drain breakdown voltage at 10.0 μA, source-to-drain leakage current at 10.0 V, and fault location (e.g., the location of a MOSFET not having reasonable electrical parameters). Based on the nature of detected faults (shorts or opens) and location, information regarding the quality of the metal step coverage, metal bridging, and other shorts or opens in the metal level can be determined.

Drawing: Figure B-27.

IV. Gate Dielectric Integrity Array (RFII) - NBS-16 and NBS-26

Purpose: The purpose of this structure is to determine the fault density of gate oxide dielectric breakdown primarily at the epi island edge.

Description: This structure contains an array of capacitors and is used to detect metal-to-poly, poly-to-epi, and metal-to-epi leakage caused by photolithography-induced defects or dielectric breakdown of the gate or field oxide. The structure is comprised of five layers on a sapphire substrate: n^- epitaxial silicon lines 0.4 mil (6 μm) wide; oxide p^+ polysilicon lines 0.4 mil (6 μm) wide running perpendicular to the epi

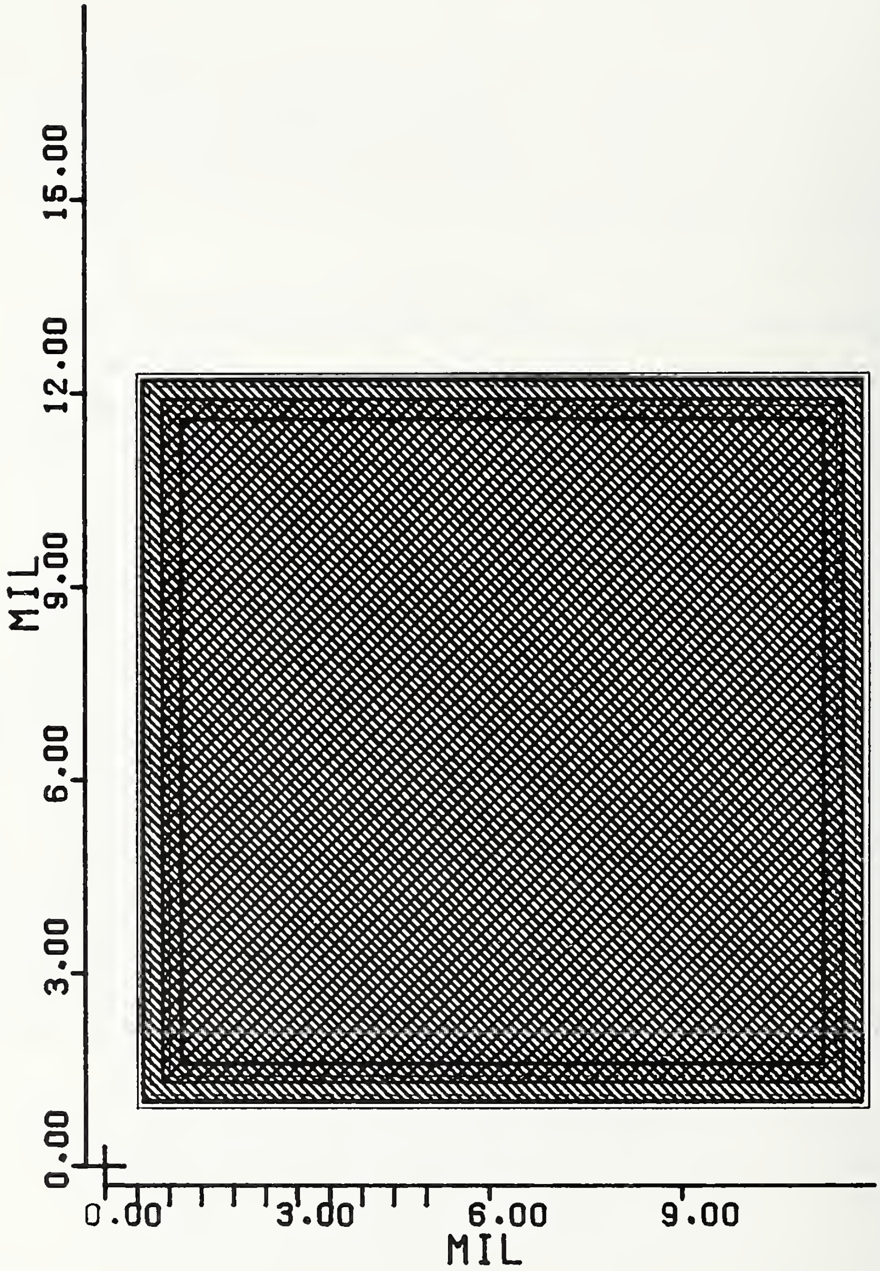


Figure B-25. SIMS area.

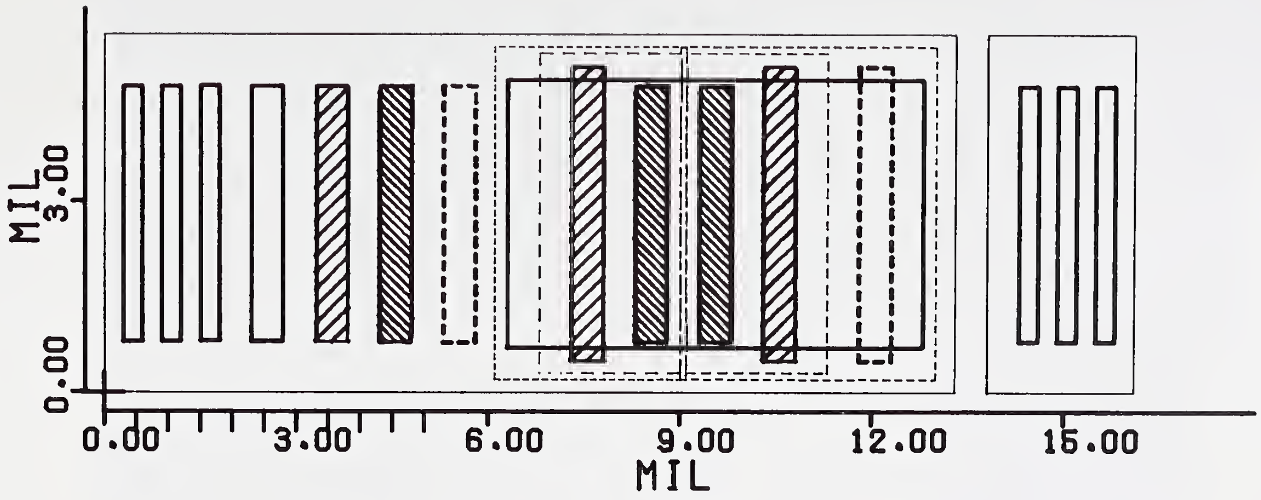
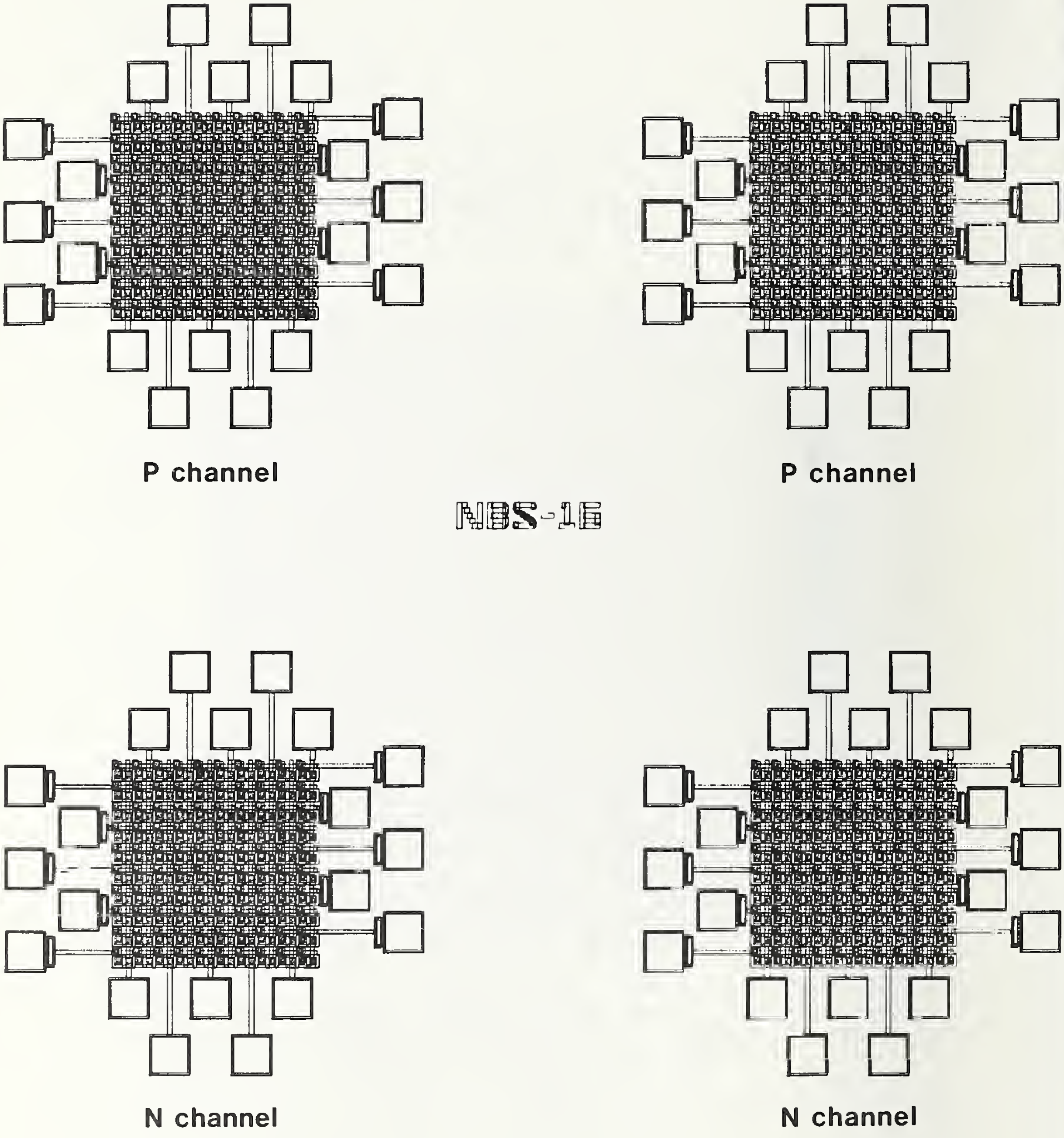


Figure B-26. Surface profilometer.



P channel

P channel

N channel

N channel

Figure B-27. Random access fault structure (RFI).

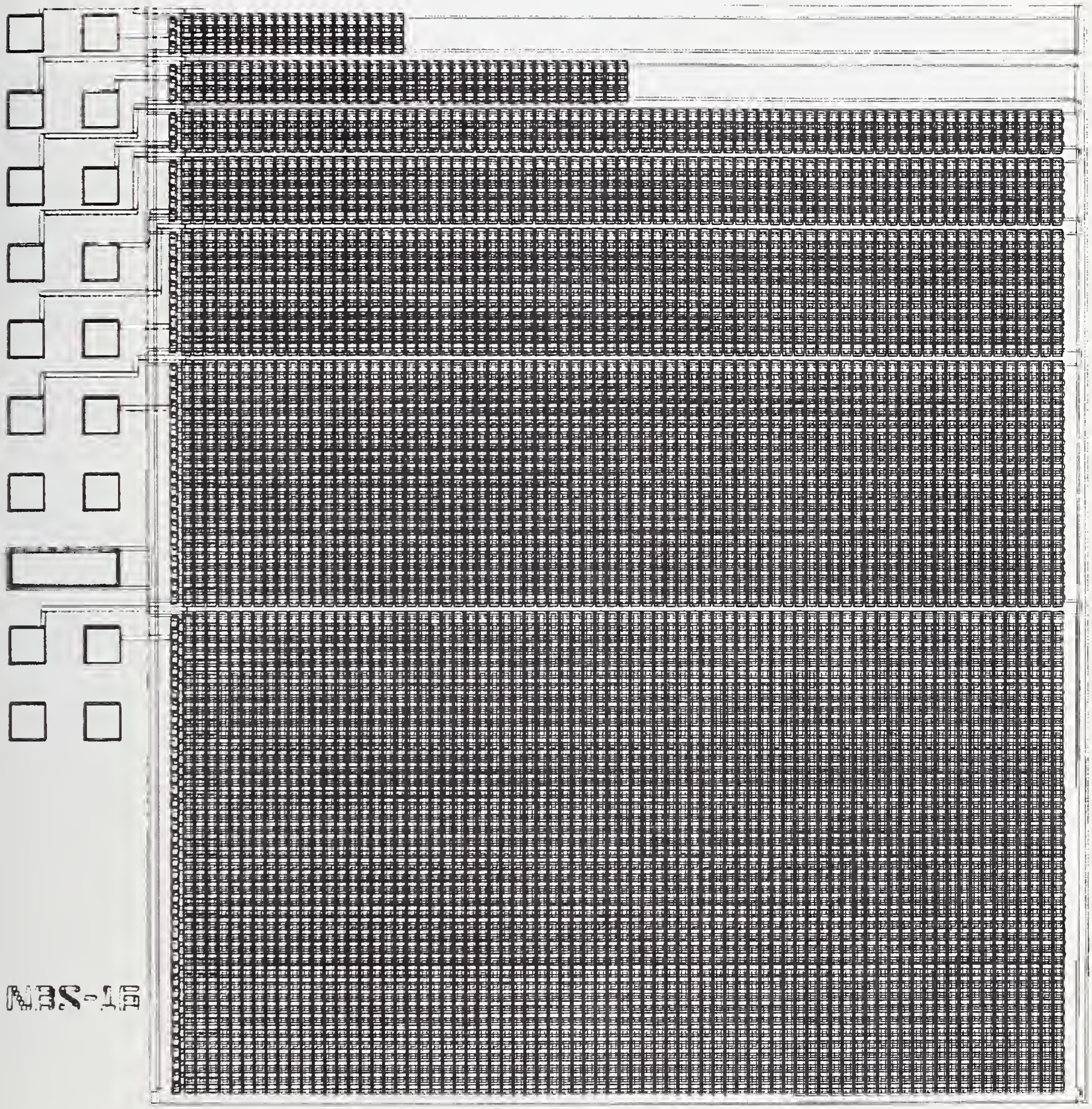


Figure B-28. Gate dielectric integrity array (RFII).

lines; field oxide; and aluminum metallization. The poly lines are grouped to form seven subarrays with 57, 114, 225, 375, 750, 1500, and 3000 crossovers. The polysilicon and metallization in each subarray are each connected to a single probe pad; all of the epi lines in all of the subarrays are electrically common and connected to a single probe pad. The array is in a 100-mil (2.54-mm) square and can be probed by a 2 by 10 probe card.

Parameters measured: Metal-to-poly, poly-to-epi, and metal-to-epi leakage current as a function of array size.

Drawing: Figure B-28.

References

B-1. *MOS Integrated Circuits*, W. M. Penney and L. Lau, Eds., pp. 126-129 (van Nostrand Co., New York, 1972).

B-2. Buehler, M. G., Grant, S. D., and Thurber, W. R., Bridge and van der Pauw Sheet Resistors for Characterizing the Line Width of Conducting Layers, *J. Electrochem. Soc.* 125, 650-654 (1978).

B-3. Buehler, M. G., *Semiconductor Measurement Technology:* Microelectronic Test Pattern NBS-3 for Evaluating the Resistivity-Dopant Density Relationship of Silicon, NBS Spec. Publ. 400-22 (June 1976).

B-4. Skorup, G. E., SOS COS/MOS Universal Array User's Manual, Solid State Technology Center, Somerville, New Jersey (May 1977).

Appendix C

VARIATION IN *p*-CHANNEL THRESHOLD VOLTAGE FOR EIGHTEEN NBS-16 PROCESS VALIDATION WAFERS

Wafer maps of *p*-channel threshold voltage for Device no. 1 from PVWs accompanying wafer lots A1 through A18 follow. The data are presented in order to show how one intrawafer parameter variation changes from lot to lot. The time interval for processing the 18 lots was about two years.

For each figure, an "×" represents the location of a measured structure having a parameter value within the eight-level gray scale used. A "+" represents the location of measured sites with parameters higher than the scale, and a "-" represents locations of measured sites lower than the scale.

Threshold voltage

(V)	No.
-0.955	
█	3
-0.905	
▓	4
-0.854	
▓	4
-0.804	
▒	8
-0.753	
▒	7
-0.703	
░	14
-0.652	
░	38
-0.602	
⠂	11
-0.552	
Sites included	89

Mean: -0.680 V
Median: -0.644 V
Standard deviation: 0.094 V

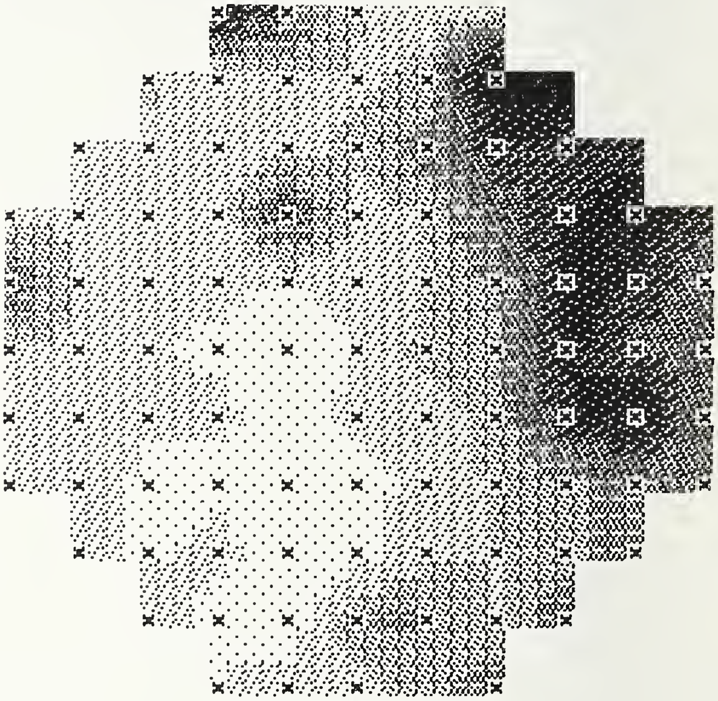


Figure C-1. Wafer map of *p*-channel threshold voltage Device no. 1, NBS-16 PVW Al.

Threshold voltage

(V)	No.
-1.324	
■	2
-1.271	
▩	2
-1.219	
▩	9
-1.166	
▦	10
-1.115	
▤	21
-1.062	
▒	22
-1.010	
░	16
-0.958	
⋯	11
-0.905	
Sites included	93

Mean: -1.063 V
Median: -1.052 V
Standard deviation: 0.089 V

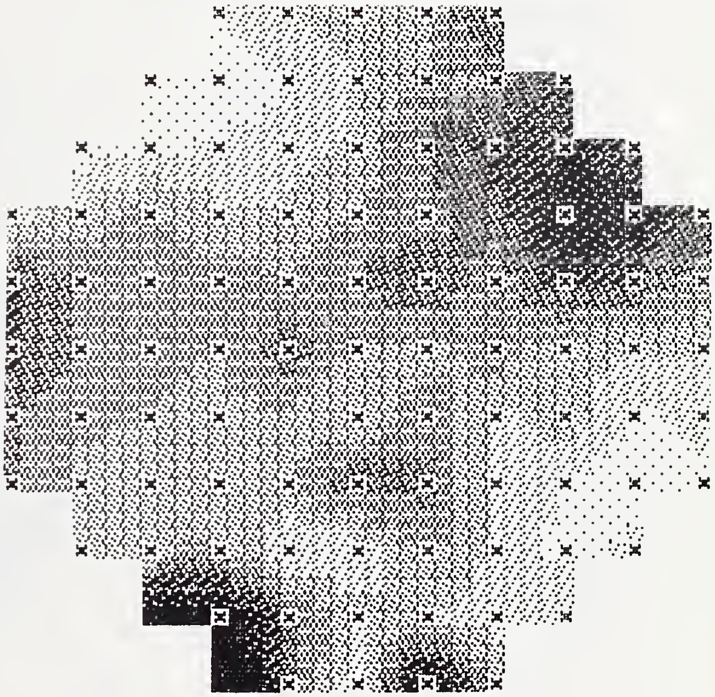


Figure C-2. Wafer map of *p*-channel threshold voltage, Device no. 1, NBS-16 PVW A2.

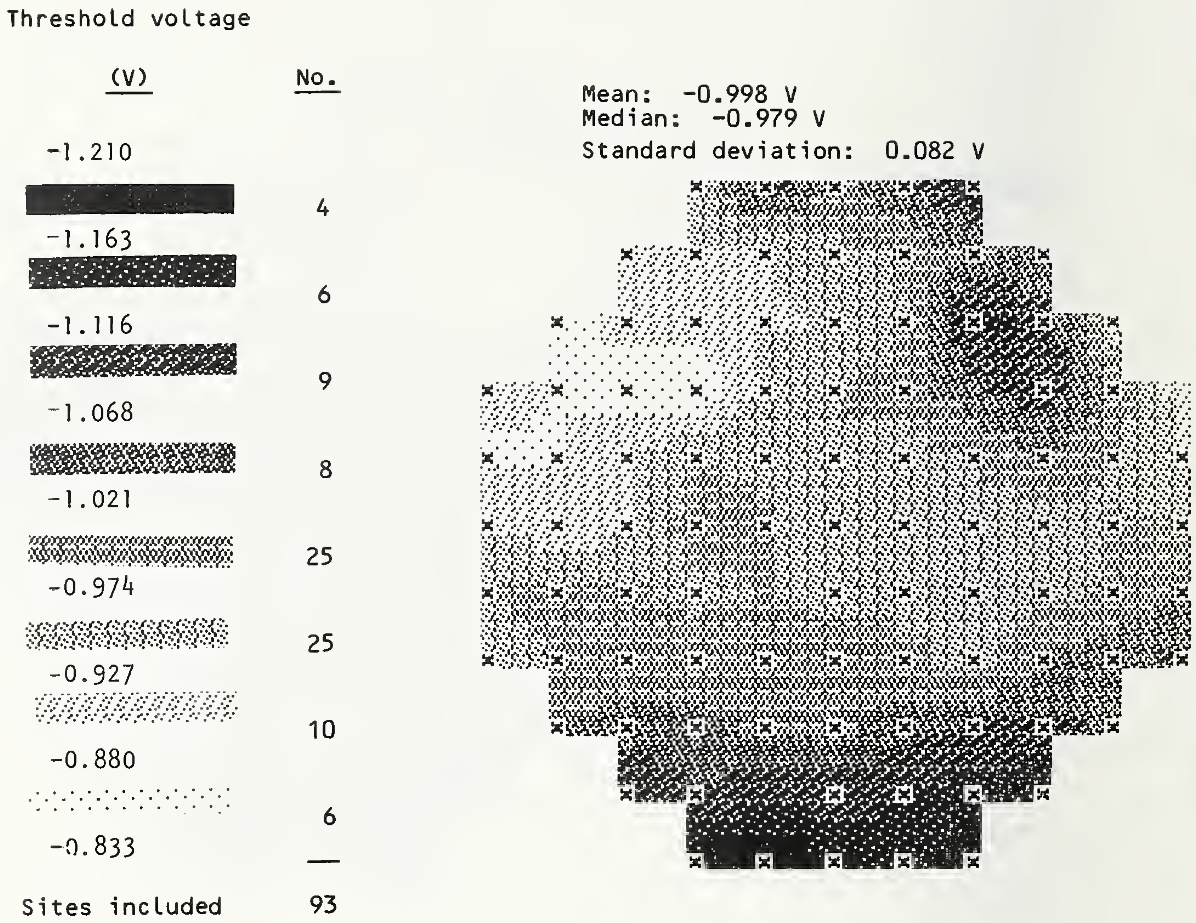


Figure C-3. Wafer map of *p*-channel threshold voltage, Device no. 1, NBS-16 PVW A3.

Threshold voltage

(V)	No.
-1.109	
█	3
-1.076	
▓	4
-1.042	
▓	6
-1.009	
▒	21
-0.975	
▒	28
-0.942	
░	15
-0.908	
░	6
-0.875	
⁚	2
-0.842	
Sites included	85

Mean: -0.967 V
Median: -0.966 V
Standard deviation: 0.048 V

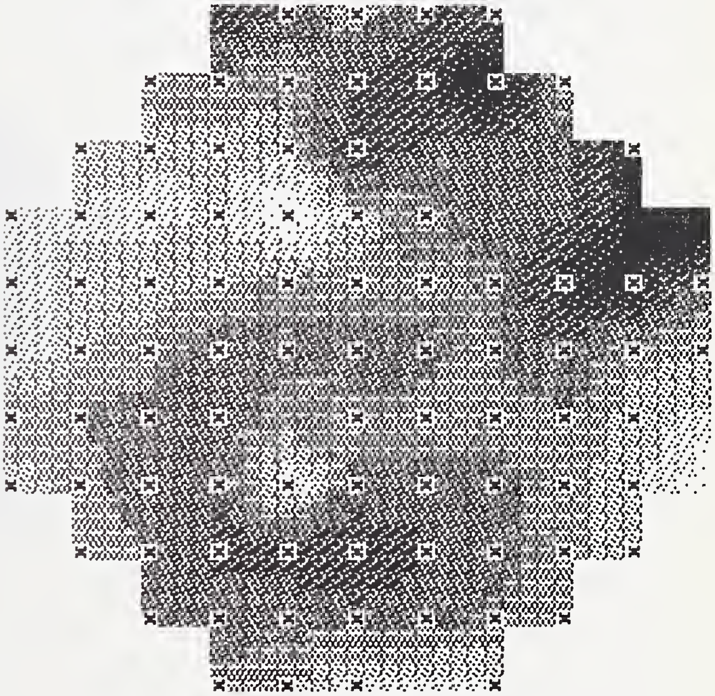


Figure C-4. Wafer map of *p*-channel threshold voltage, Device no. 1, NBS-16 PVW A4.

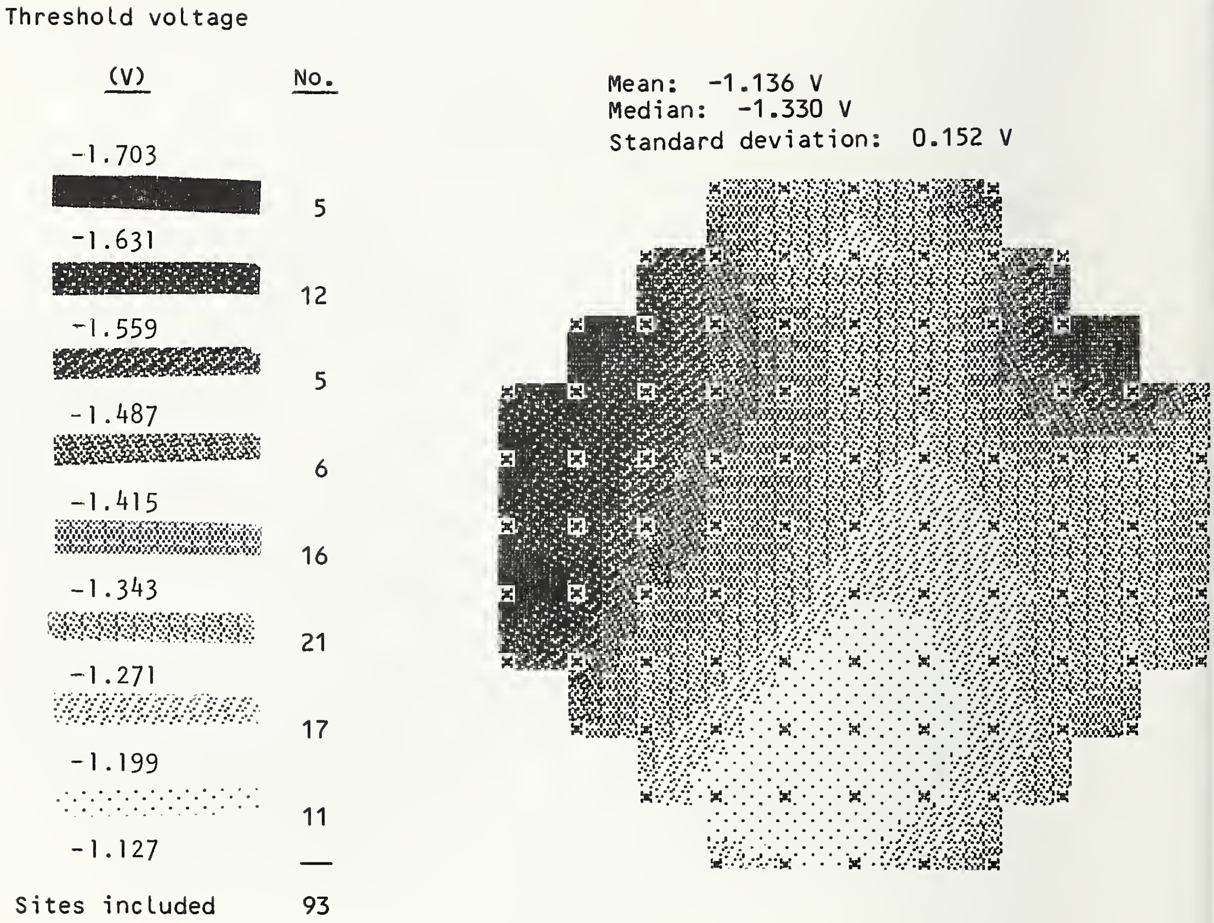


Figure C-5. Wafer map of *p*-channel threshold voltage, Device no. 1, NBS-16 PVW A5.

Threshold voltage

(V)	No.
-1.171	
█	3
-1.134	
▓	3
-1.096	
▓	4
-1.059	
▒	18
-1.022	
▒	9
-0.984	
░	18
-0.947	
░	22
-0.909	
⋯	13
-0.872	
Sites included	90

Mean: -0.983 V
Median: -0.969 V
Standard deviation: 0.069 V

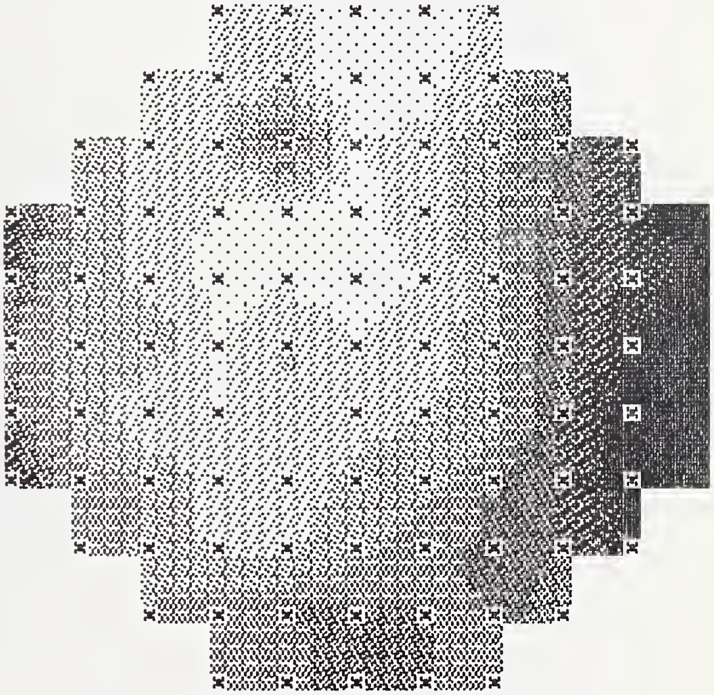


Figure C-6. Wafer map of *p*-channel threshold voltage, Device no. 1, NBS-16 PVW A6.

Threshold voltage

(V)	No.
-1.203	
■	5
-1.159	
▩	4
-1.115	
▨	4
-1.071	
▨	5
-1.026	
▦	18
-0.982	
▤	33
-0.938	
░	16
-0.894	
⁘	3
-0.850	
Sites included	88

Mean: -0.990 V
Median: -0.976 V
Standard deviation: 0.073 V

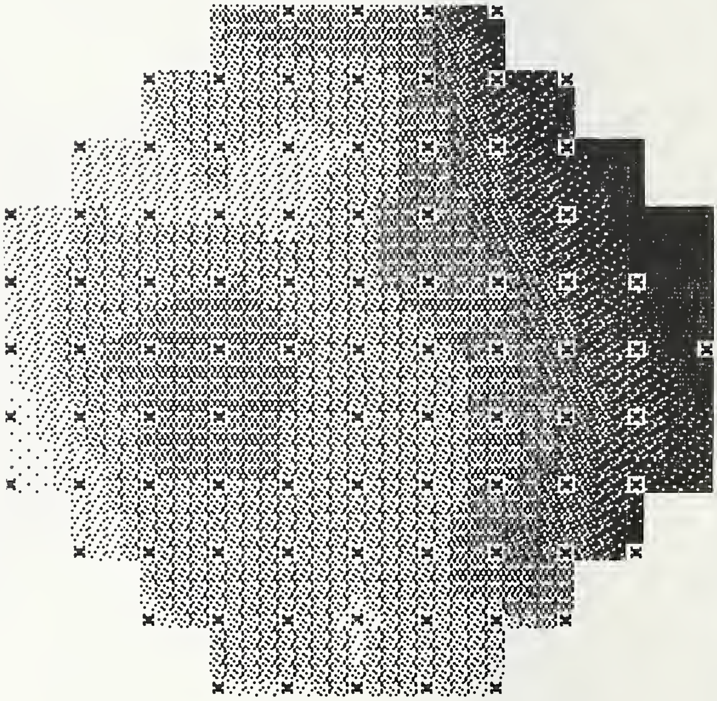


Figure C-7. Wafer map of *p*-channel threshold voltage, Device no. 1, NBS-16 PVW A7.

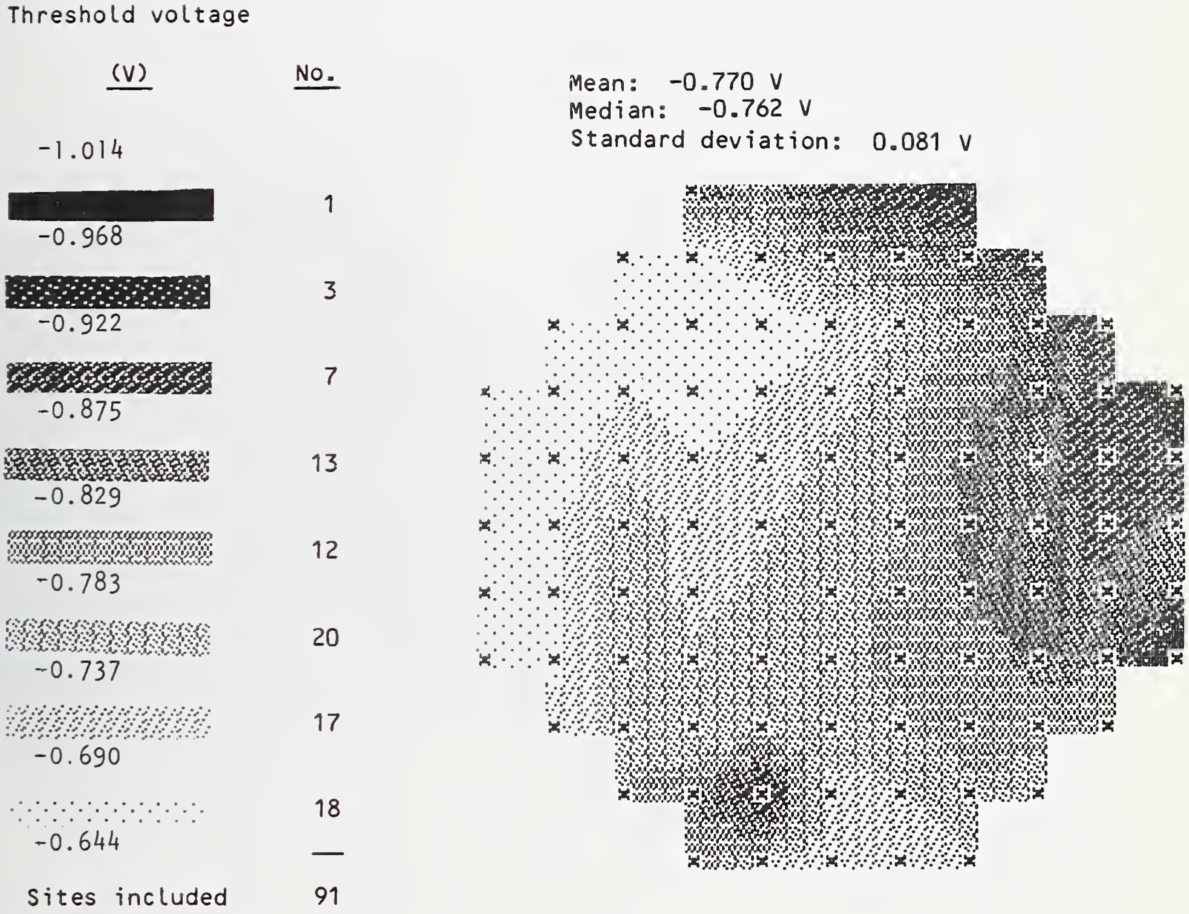


Figure C-8. Wafer map of *p*-channel threshold voltage, Device no. 1, NBS-16 PVW A8.

Threshold voltage

(V)		No.
-0.865		
	■	9
-0.806		
	▩	11
-0.747		
	▦	15
-0.689		
	▨	13
-0.630		
	▧	15
-0.571		
	▤	13
-0.513		
	░	11
-0.454		
	⋯	4
-0.396		—
Sites included		91

Mean: -0.646 V
Median: -0.639 V
Standard deviation: 0.118 V

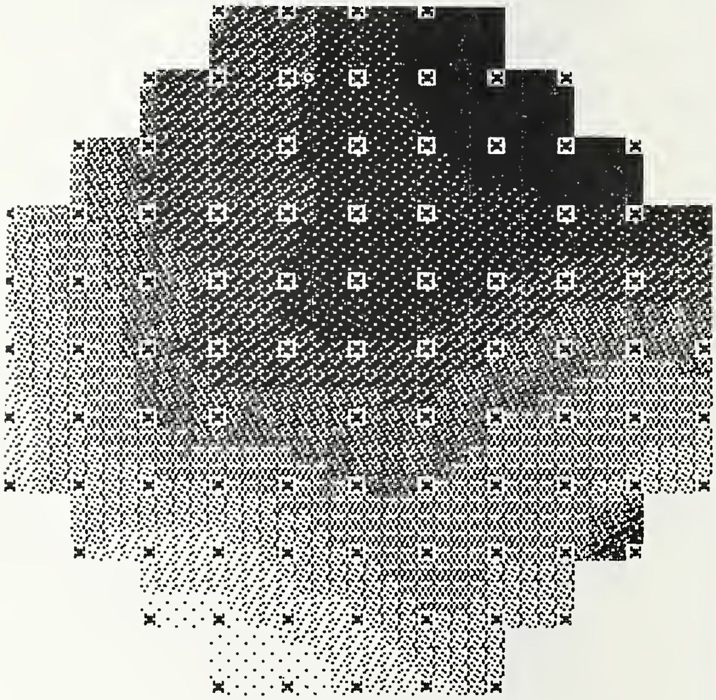


Figure C-9. Wafer map of *p*-channel threshold voltage, Device no. 1, NBS-16 PVW A9.

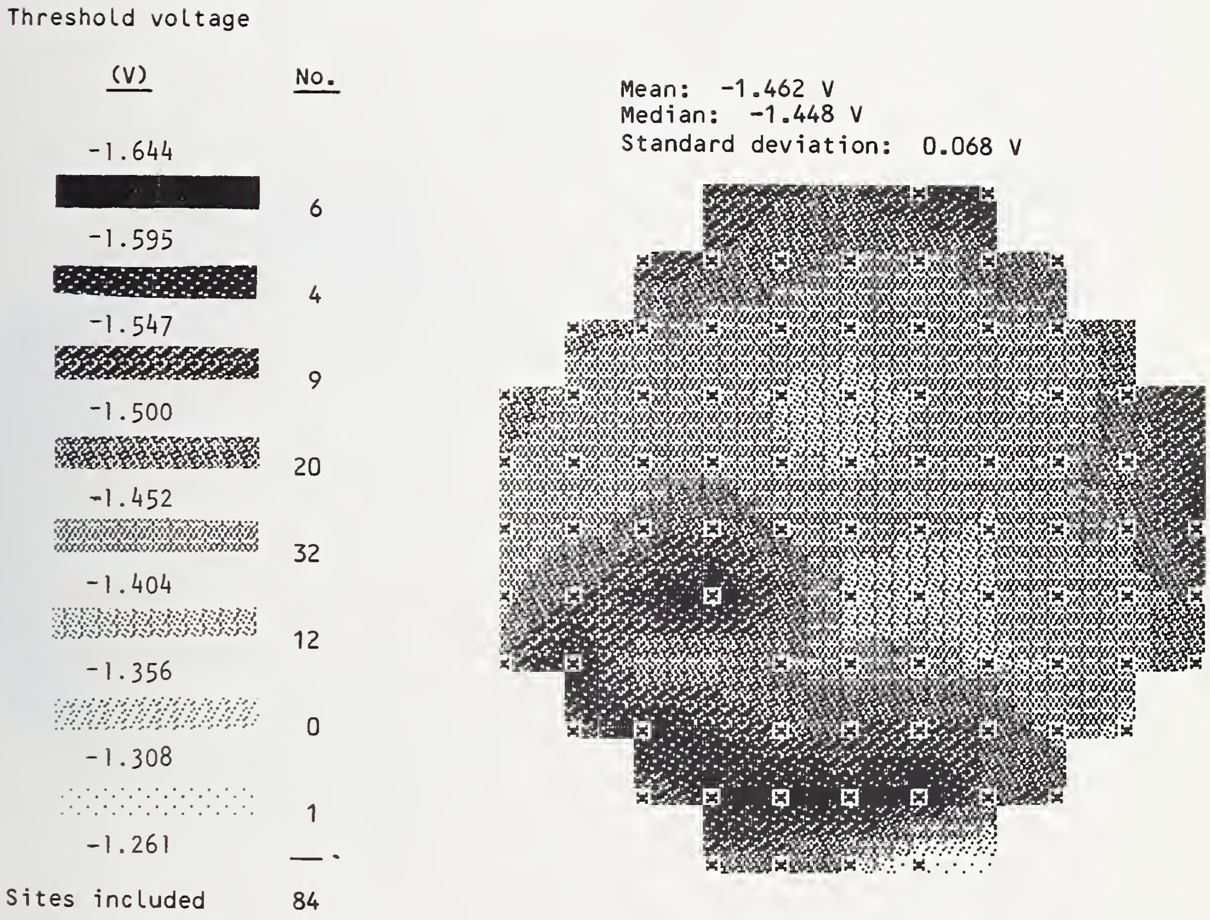


Figure C-10. Wafer map of *p*-channel threshold voltage, Device no. 1, NBS-16 PVW A10.

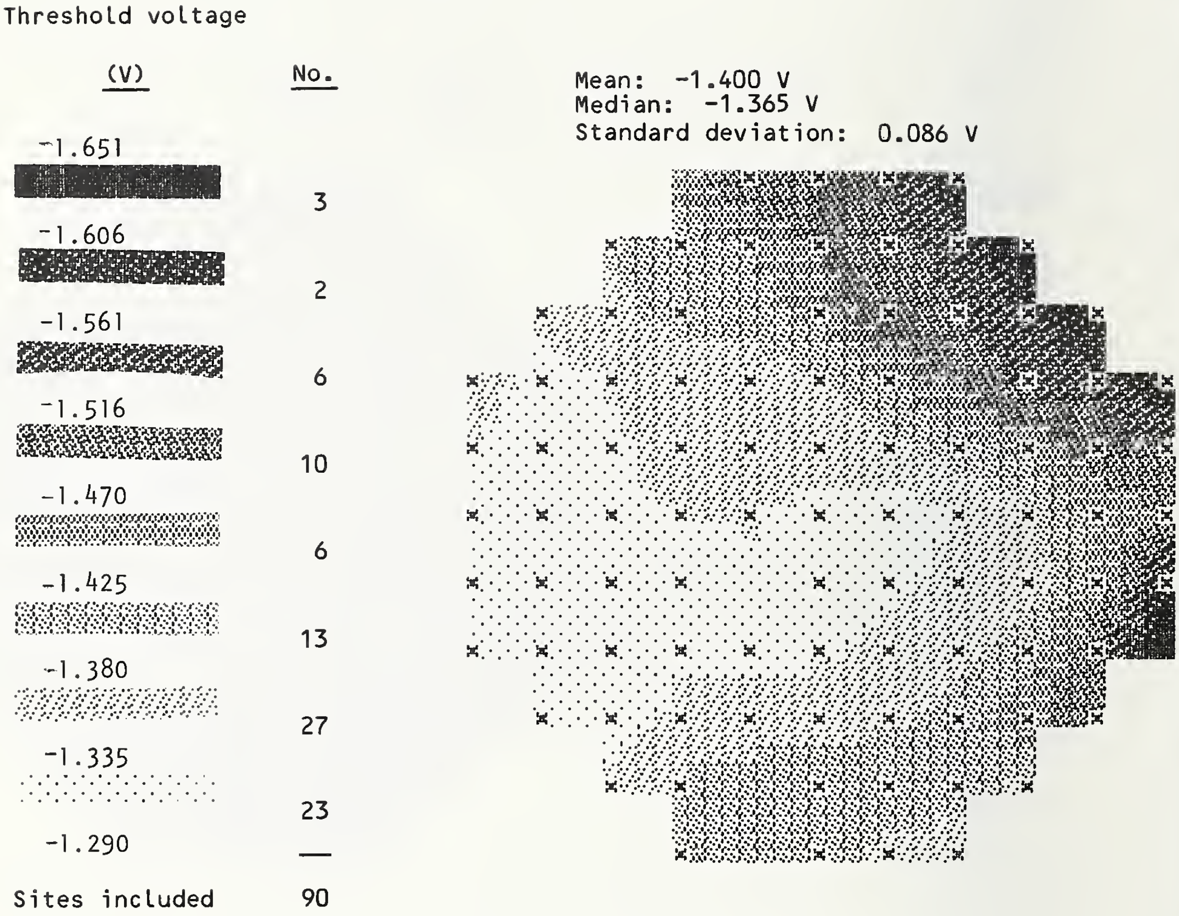


Figure C-11. Wafer map of p-channel threshold voltage, Device no. 1, NBS-16 PVW All.

Threshold voltage

(V)	No.
-1.236	
■	3
-1.193	
▓	5
-1.150	
▓	6
-1.107	
▒	5
-1.064	
▒	23
-1.021	
░	17
-0.979	
░	8
-0.936	
⋯	15
-0.893	—
Sites included	82

Mean: -1.026 V
Median: -1.024 V
Standard deviation: 0.084 V

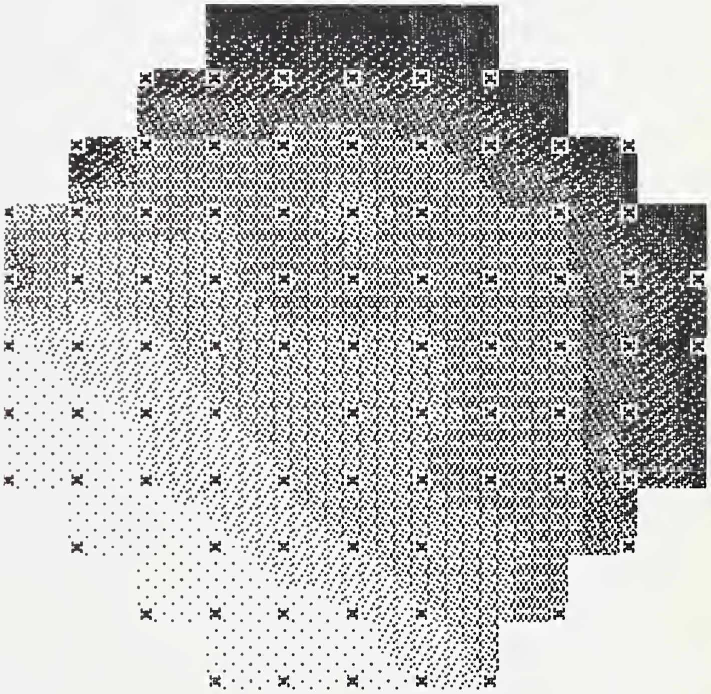


Figure C-12. Wafer map of *p*-channel threshold voltage, Device no. 1, NBS-16 PVW A12.

Threshold voltage (V)	No.
-1.591	
■	2
-1.510	
▓	0
-1.430	
▓	8
-1.349	
▒	18
-1.268	
▒	9
-1.187	
░	10
-1.107	
░	14
-1.026	
⋅	32
-0.946	
Sites included	93

Mean: -1.145 V
Median: -1.107 V
Standard deviation: 0.157 V

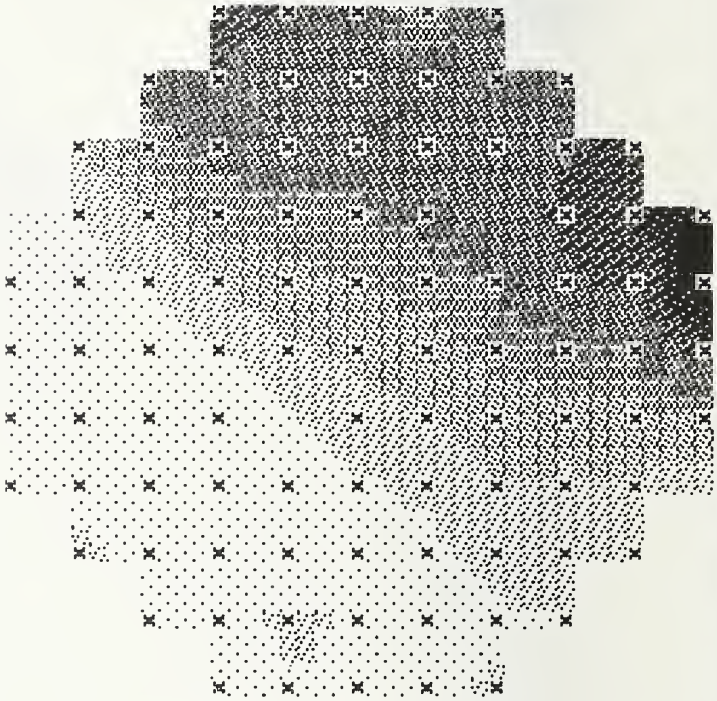


Figure C-13. Wafer map of *p*-channel threshold voltage, Device no. 1, NBS-16 PVW A13.

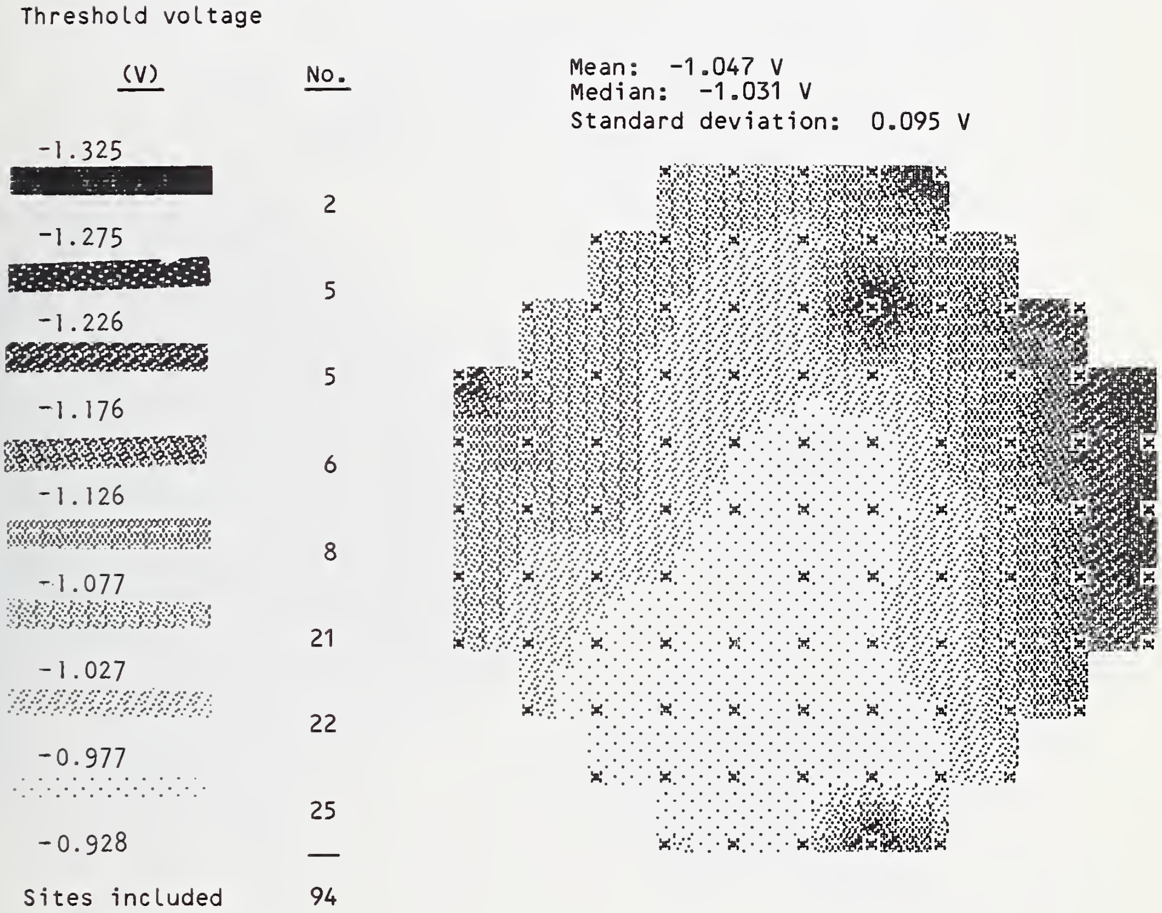


Figure C-14. Wafer map of *p*-channel threshold voltage, Device no. 1, NBS-16 PVW A14.

Threshold voltage

(V)		No.
-1.139		
	█	4
-1.085		
	▓	11
-1.032		
	▓	20
-0.978		
	▒	19
-0.925		
	▒	9
-0.872		
	░	17
-0.818		
	░	10
-0.764		
	·	4
-0.711		
Sites included		94

Mean: -0.932 V
Median: -0.957 V
Standard deviation: 0.100 V

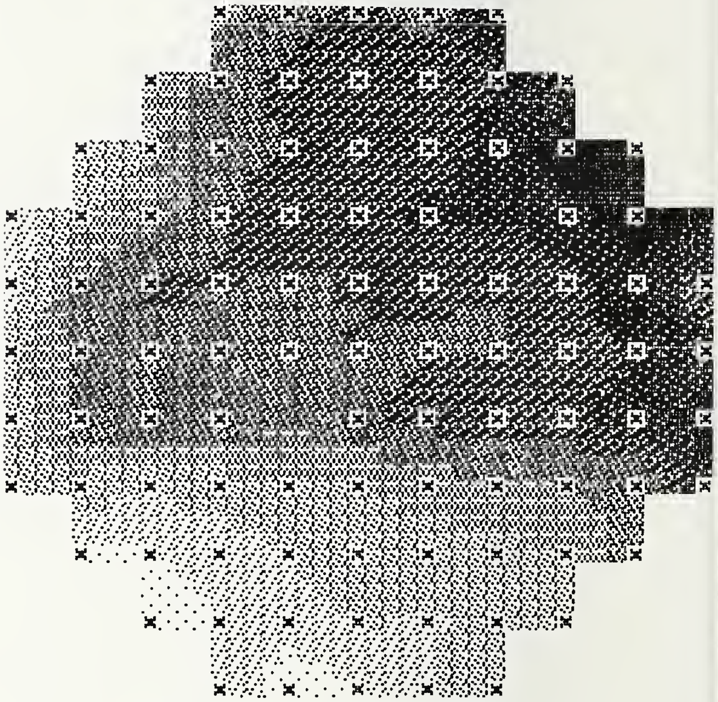


Figure C-15. Wafer map of *p*-channel threshold voltage, Device no. 1, NBX-16 PVW A15.

Threshold voltage

(V)	No.
-0.876	
■	5
-0.854	
▩	3
-0.832	
▦	1
-0.811	
▨	5
-0.789	
▒	12
-0.789	
▒	17
-0.768	
░	16
-0.746	
░	23
-0.703	—
Sites included	82

Mean: -0.757 V
Median: -0.747 V
Standard deviation: 0.042 V

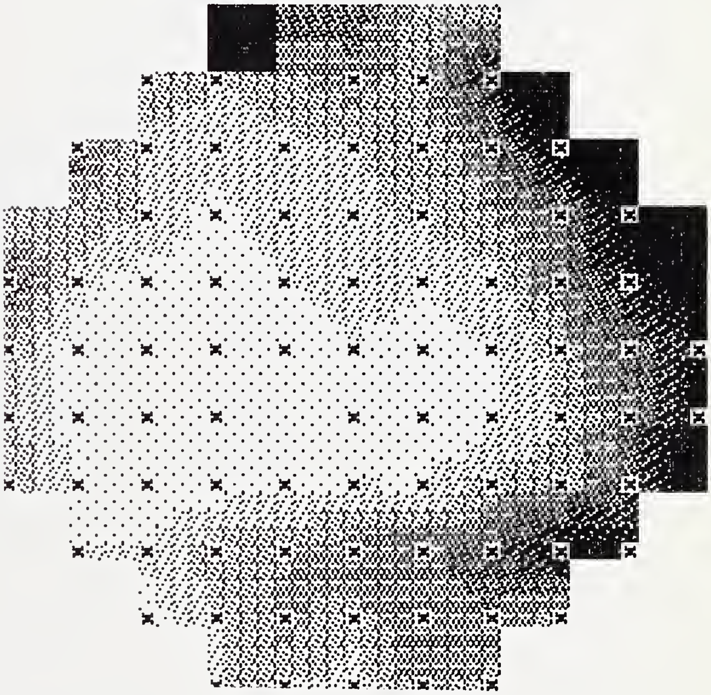
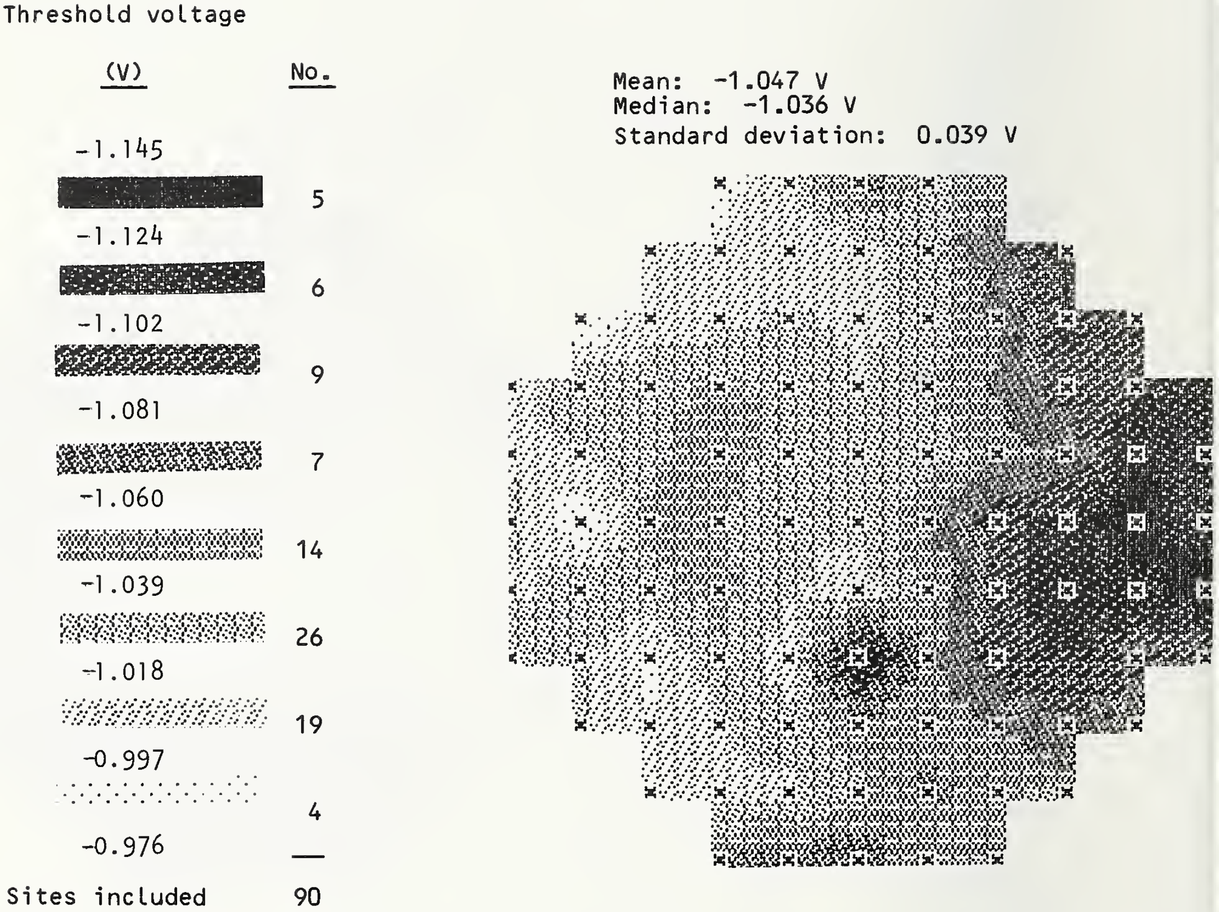
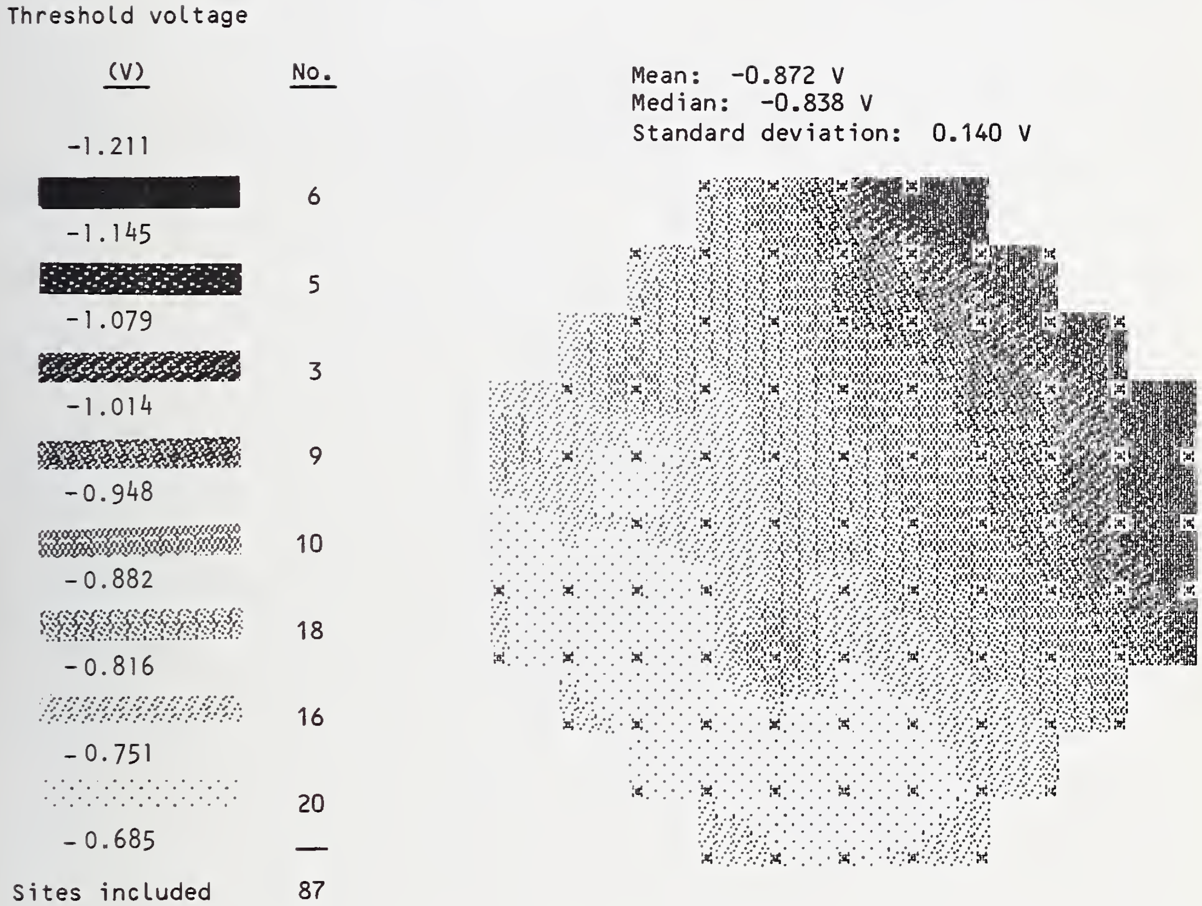


Figure C-16. Wafer map of *p*-channel threshold voltage, Device no. 1, NBS-16 PVW A16.



Mean: -1.047 V
Median: -1.036 V
Standard deviation: 0.039 V

Figure C-17. Wafer map of *p*-channel threshold voltage, Device no. 1, NBS-16 PVW A17.



Threshold voltage

(V)		No.
-1.211		
	■	6
-1.145		
	▩	5
-1.079		
	▩	3
-1.014		
	▨	9
-0.948		
	▨	10
-0.882		
	▧	18
-0.816		
	▧	16
-0.751		
	⁚	20
-0.685		—
Sites included		87

Mean: -0.872 V
Median: -0.838 V
Standard deviation: 0.140 V

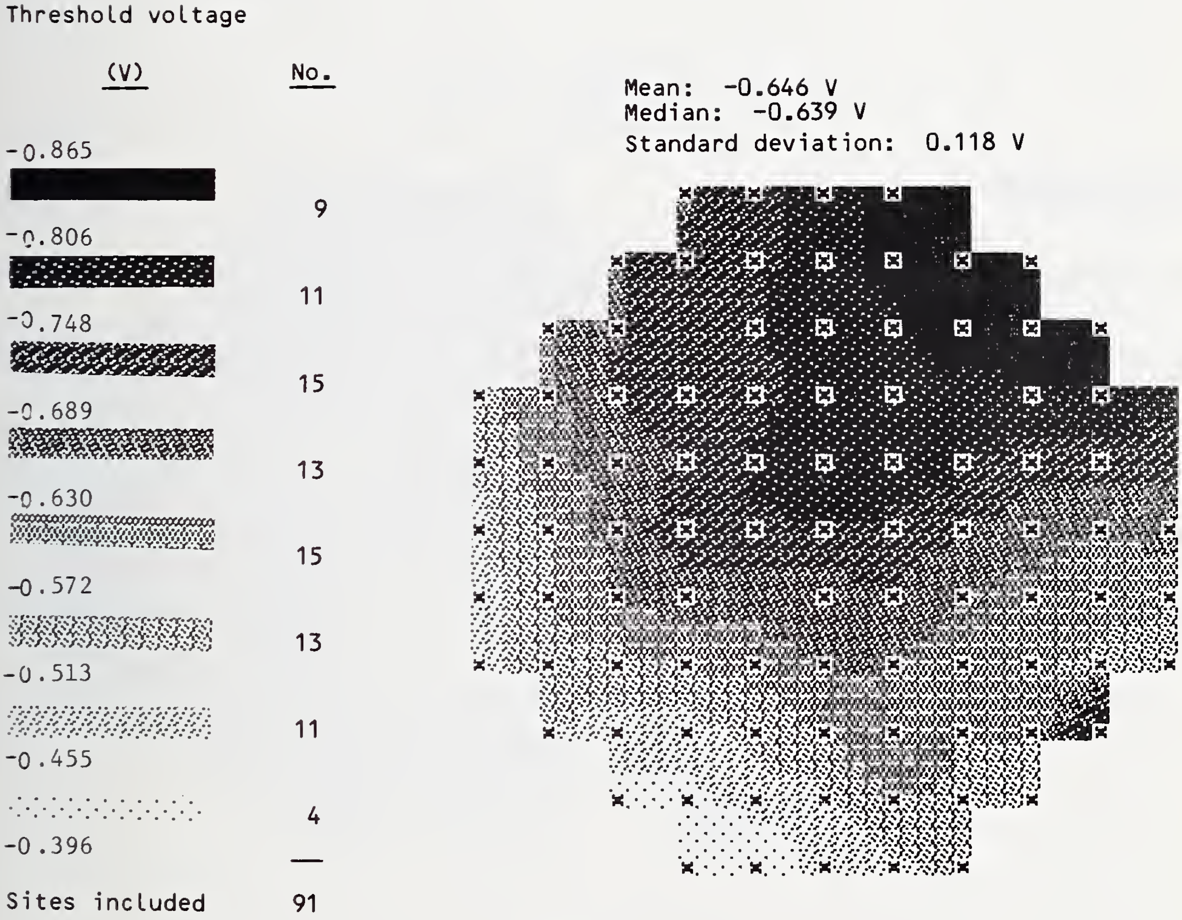
Figure C-18. Wafer map of *p*-channel threshold voltage, Device no. 1, NBS-16 PVW A18.

Appendix D

CRITICAL ELECTRICAL PARAMETERS FROM ONE NBS-16 PROCESS VALIDATION WAFER

Wafer maps of critical electrical process parameters from the PVW accompanying wafer lot A9 follow. The data presented are from test structures found in the process parameter pattern and are typical of data found on other PVWs. The data are presented in order to show the type of information that can be obtained from one PVW.

For each figure, an "×" represents the location of a measured structure having a parameter value within the eight-level gray scale used. A "+" represents the location of measured sites with parameters higher than the scale, and a "-" represents locations of measured sites lower than the scale.



Mean: -0.646 V
Median: -0.639 V
Standard deviation: 0.118 V

Figure D-1. Wafer map of *p*-channel threshold voltage, Device no. 1.

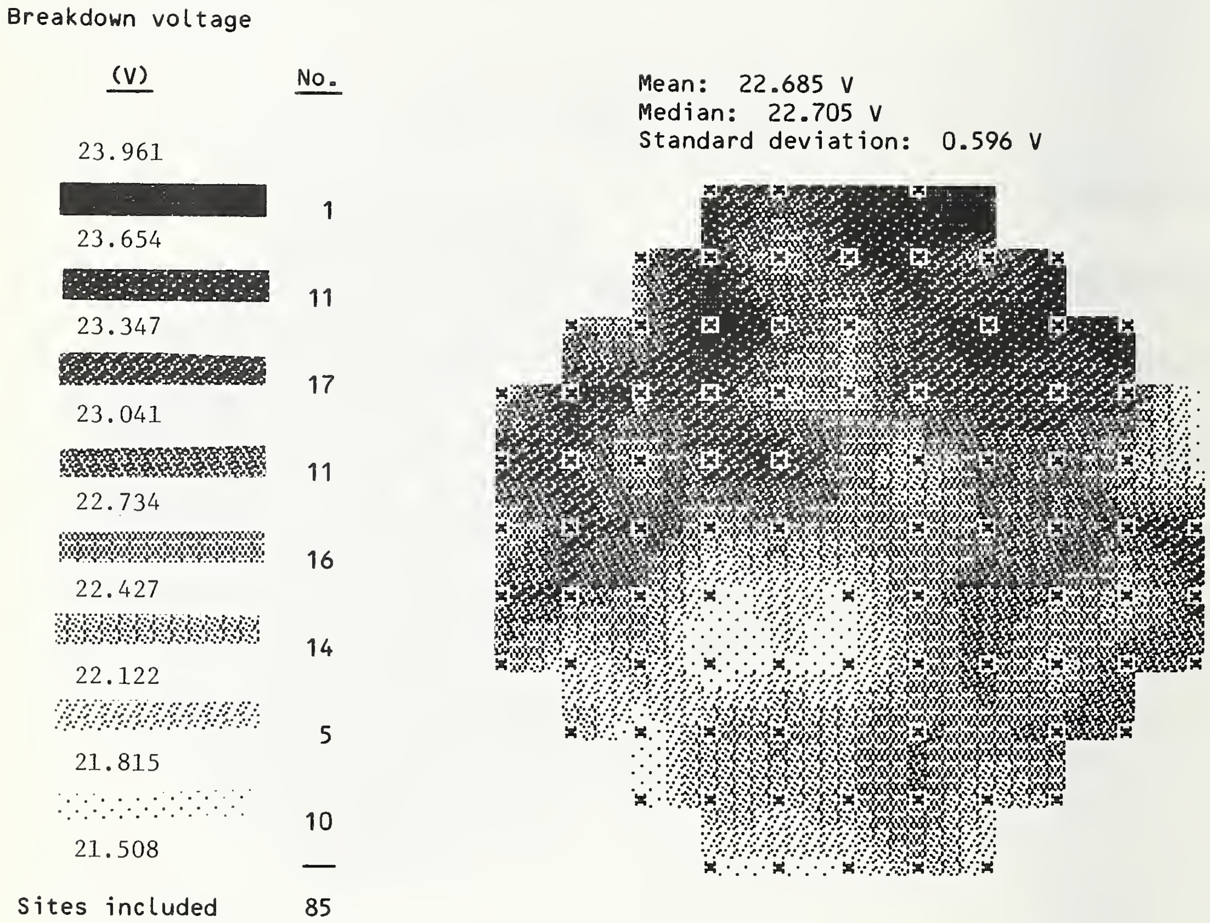
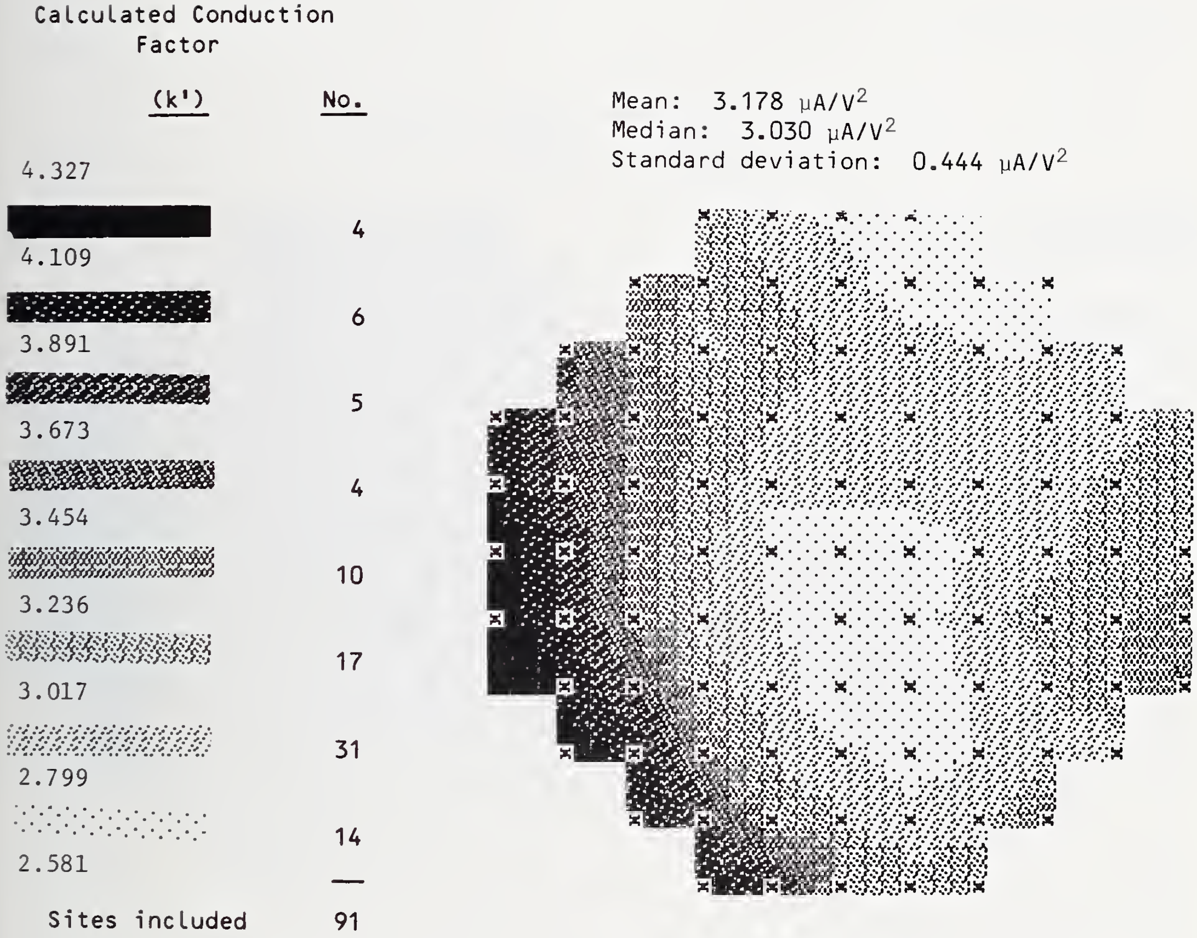


Figure D-2. Wafer map of *p*-channel breakdown voltage, Device no. 1.



Mean: 3.178 $\mu A/V^2$
Median: 3.030 $\mu A/V^2$
Standard deviation: 0.444 $\mu A/V^2$

Figure D-3. Wafer map of *p*-channel calculated conduction factor, Device no. 1.

Calculated Threshold
Voltage

(V)		No.
0.679		
	█	9
0.624		
	▓	11
0.569		
	▨	16
0.514		
	▦	11
0.459		
	▒	14
0.404		
	░	17
0.349		
	⁘	9
0.294		
	·	4
0.239		
Sites included		91

Mean: 0.472 V
Median: 0.468 V
Standard deviation: 0.111 V

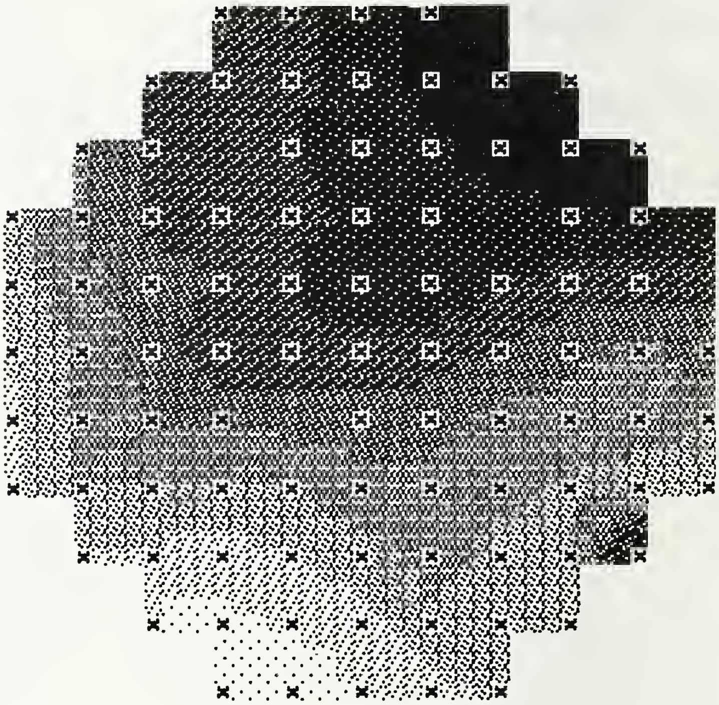


Figure D-4. Wafer map of *p*-channel calculated threshold voltage, Device no. 1.

Threshold Voltage

(V)		No.
2.913		
	■	6
2.847		
	▩	3
2.781		
	▩	6
2.715		
	▦	11
2.649		
	▦	22
2.583		
	▨	24
2.516		
	▨	13
2.450		
	░	4
2.384		
Sites included		89

Mean: 2.610 V
Median: 2.592 V
Standard deviation: 0.117 V

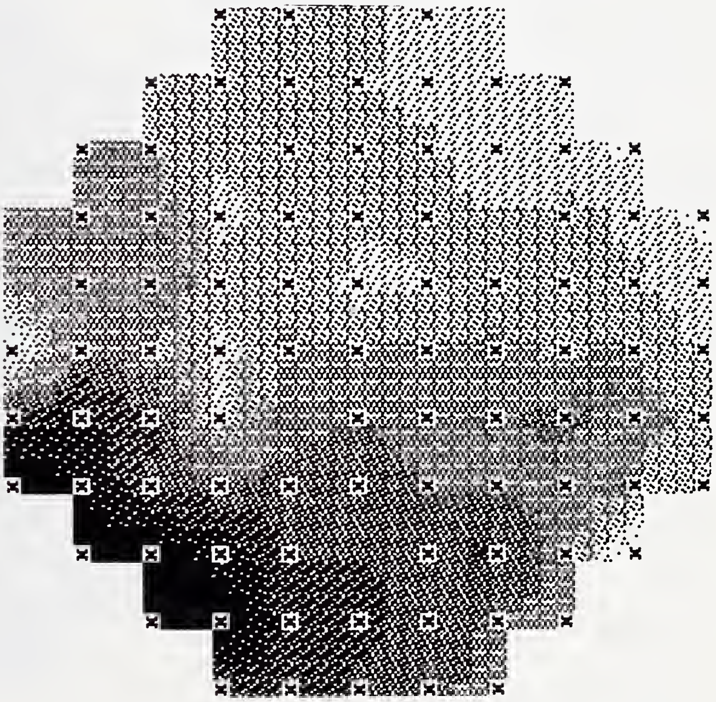


Figure D-5. Wafer map of *n*-channel threshold voltage, Device no. 2.

Breakdown Voltage

(V)	No.
20.646	
■	10
20.409	
▩	23
20.171	
▩	14
19.934	
▦	15
19.697	
▦	7
19.460	
▨	8
19.222	
░	3
18.985	
⋯	2
18.748	
Sites included	82

Mean: 19.957 V
Median: 20.037 V
Standard deviation: 0.437 V

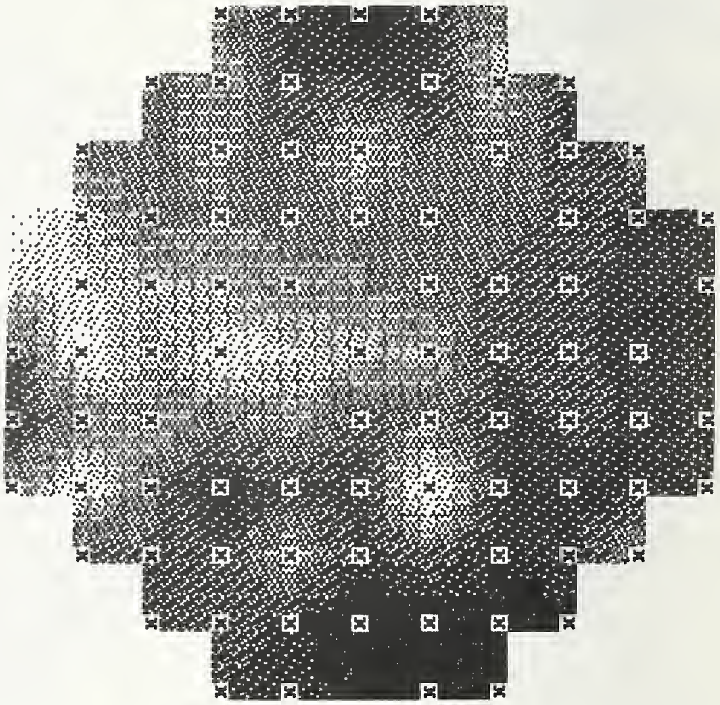


Figure D-6. Wafer map of *n*-channel breakdown voltage, Device no. 2.

Calculated Conduction
Factor

(k')		No.
7.522		
	■	2
6.582		
	▩	7
5.641		
	▦	8
4.701		
	▓	4
3.762		
	▒	10
2.821		
	▨	12
1.881		
	░	14
.941		
	⁚	34
.001		
Sites included		91

Mean: 2.309 μA/V^2
Median: 1.640 μA/V^2
Standard deviation: 2.054 μA/V^2

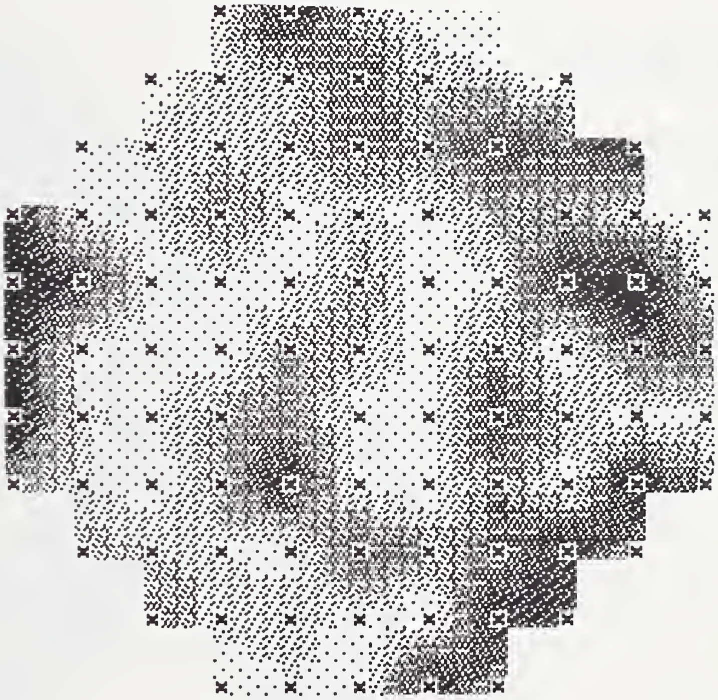


Figure D-7. Wafer map of *n*-channel calculated conduction factor, Device no. 2.

Calculated Threshold Voltage

(V)	No.
5.536	
█	3
5.010	
▓	7
4.483	
▓	28
3.957	
▓	14
3.430	
▒	5
2.904	
▒	29
2.377	
░	2
1.851	
░	2
1.324	
Sites included	90

Mean: 3.553 V
Median: 3.684 V
Standard deviation: 0.878 V

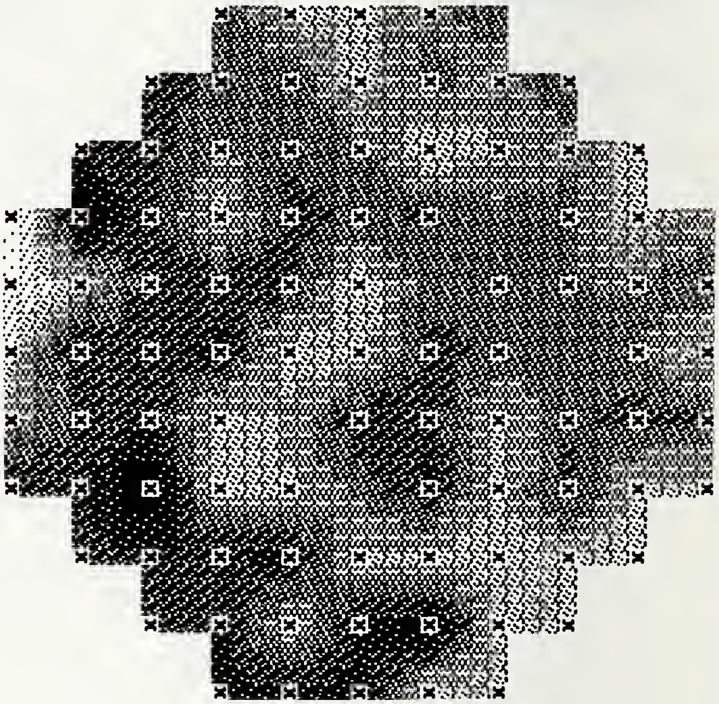


Figure D-8. Wafer map of *n*-channel calculated threshold voltage, Device no. 2.

Threshold Voltage

(V)		No.
2.821		
	■	4
2.783		
	▩	10
2.745		
	▨	15
2.707		
	▦	31
2.668		
	▤	11
2.630		
	▧	7
2.592		
	▥	7
2.554		
	░	1
2.516		
Sites included		86

Mean: 2.685 V
Median: 2.691 V
Standard deviation: 0.059 V

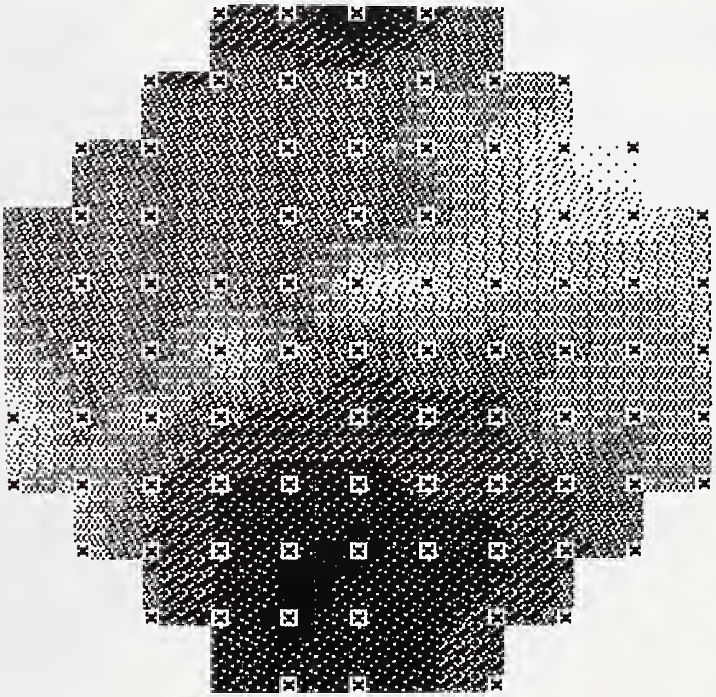


Figure D-9. Wafer map of *n*-channel threshold voltage, Device no. 3.

Breakdown Voltage

(V)		No.
21.563		
	█	7
19.700		
	▓	42
17.837		
	▓	14
15.975		
	▒	8
14.112		
	▒	7
12.249		
	░	13
10.387		
	░	1
8.524		
	⋯	2
6.661		
Sites included		94

Mean: 16.685 V
Median: 18.179 V
Standard deviation: 3.379 V

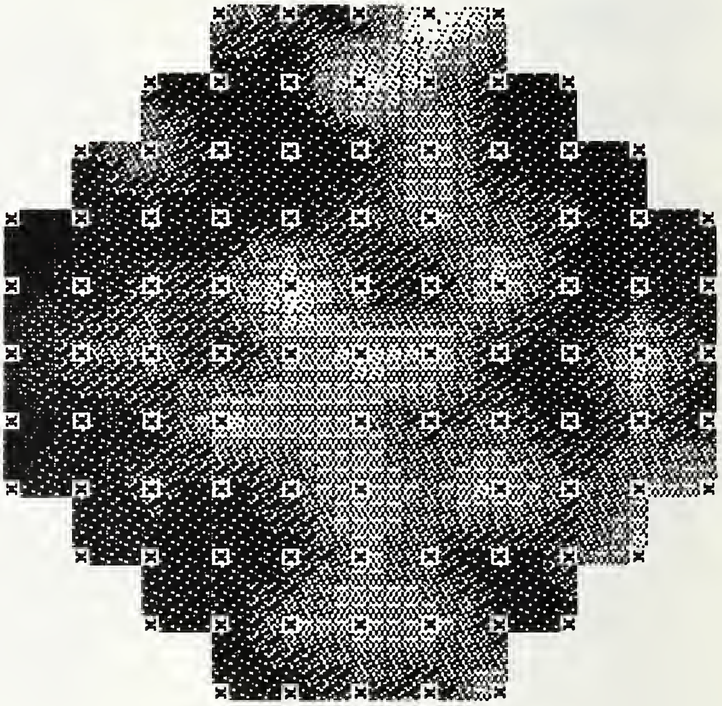


Figure D-10. Wafer map of *n*-channel breakdown voltage, Device no. 3.

Calculated Conduction
Factor

(k')	No.
4.975	
■	4
4.397	
▩	6
3.819	
▦	4
3.241	
▨	9
2.664	
▒	54
2.086	
▒	11
1.507	
░	0
0.929	
░	3
0.352	
Sites included	91

Mean: 2.607 $\mu A/V^2$
Median: 2.519 $\mu A/V^2$
Standard deviation: 0.817 $\mu A/V^2$

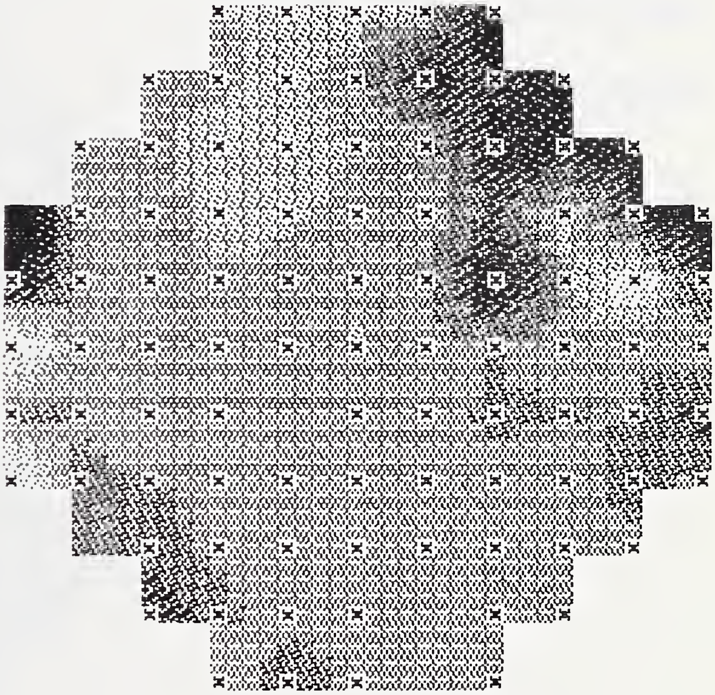


Figure D-11. Wafer map of *n*-channel calculated conduction factor, Device no. 3.

Calculated Threshold
Voltage

(V)	No.
2.754	
■	6
2.724	
▩	7
2.695	
▩	10
2.666	
▨	19
2.636	
▨	20
2.607	
▒	9
2.577	
░	5
2.548	
⁘	4
2.519	
Sites included	80

Mean: 2.641 V
Median: 2.639 V
Standard deviation: 0.0531 V

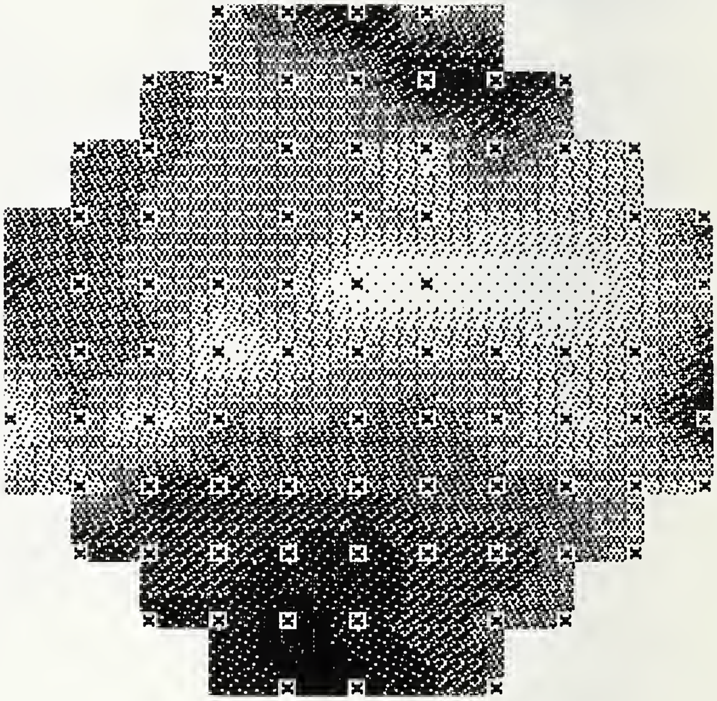


Figure D-12. Wafer map of *n*-channel calculated threshold voltage, Device no. 3.

Threshold Voltage

(V)	No.
-1.021	
■	5
- 0.950	
▩	10
- 0.880	
▦	11
- 0.809	
▨	14
- 0.739	
▧	20
- 0.668	
▤	17
- 0.598	
░	10
- 0.527	
⋯	4
- 0.457	—
Sites included	91

Mean: -0.735 V
Median: -0.716 V
Standard deviation: 0.137 V

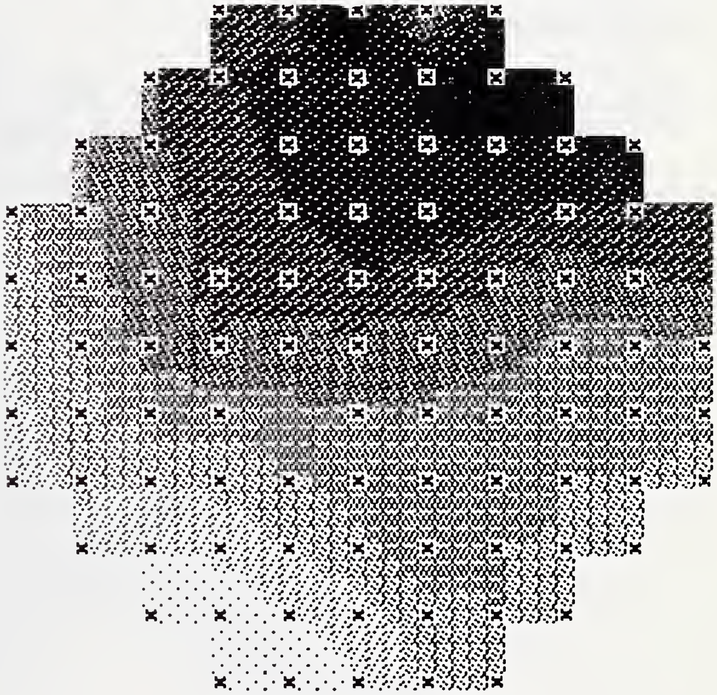


Figure D-13. Wafer map of *p*-channel threshold voltage, Device no. 4.

Breakdown Voltage

(V)	No.
24.904	
█	4
24.157	
▓	14
23.410	
▓	33
22.663	
▒	15
21.916	
▒	5
21.169	
░	5
20.423	
░	1
19.676	
⋯	2
18.929	
Sites included	79

Mean: 22.768 V
Median: 23.003 V
Standard deviation: 1.074 V

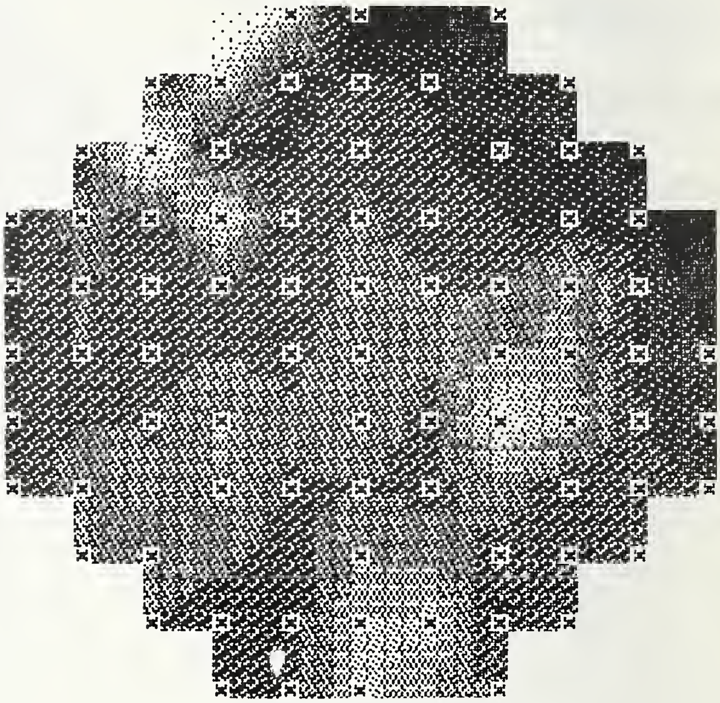


Figure D-14. Wafer map of *p*-channel breakdown voltage, Device no. 4.

Calculated Conduction
Factor

(k')	No.
3.946	
■	5
3.726	
▓	5
3.506	
▓	6
3.285	
▒	7
3.066	
▒	13
2.845	
░	30
2.625	
░	20
2.405	
⋯	6
2.185	—
Sites included	92

Mean: 2.885 μA/V^2
Median: 2.749 μA/V^2
Standard deviation: 0.408 μA/V^2

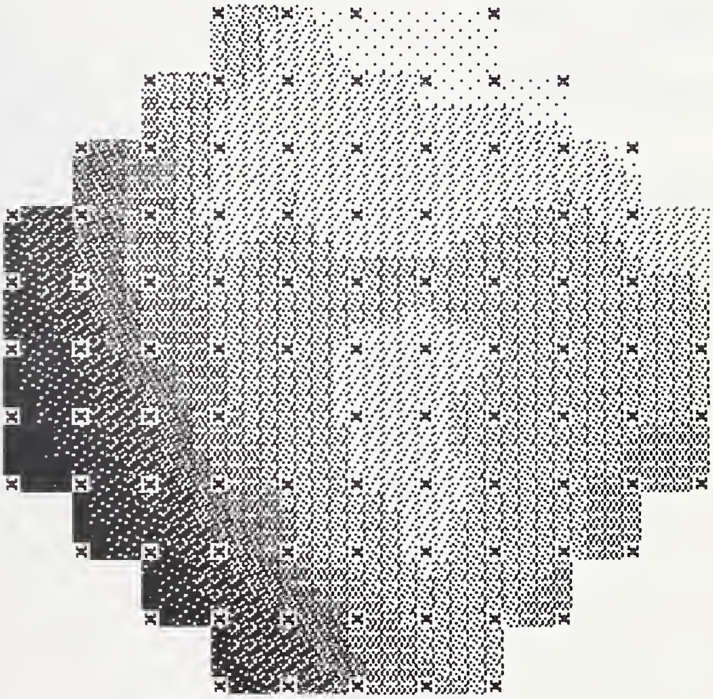


Figure D-15. Wafer map of *p*-channel calculated conduction factor, Device no. 4.

Calculated Threshold
Voltage

(V)	No.
0.825	
█	6
0.759	
▓	12
0.693	
▓	9
0.627	
▒	14
0.561	
▒	17
0.495	
░	21
0.429	
░	8
0.363	
⋯	4
0.297	
Sites included	91

Mean: 0.561 V
Median: 0.548 V
Standard deviation: 0.129 V

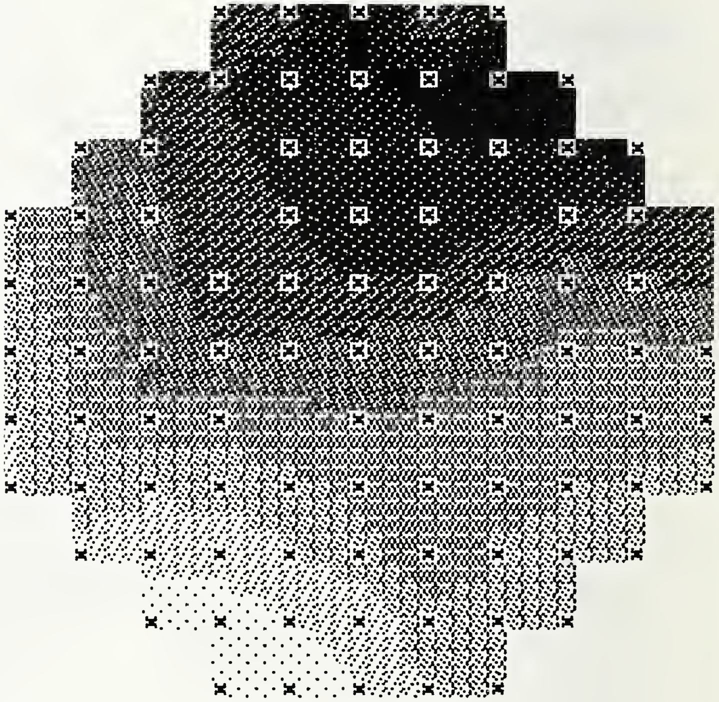


Figure D-16. Wafer map of *p*-channel calculated threshold voltage, Device no. 4.

Resistance (Ω/□)		No.
111.360		
	■	5
105.994		
	■	8
100.627		
	▩	8
95.261		
	▩	7
89.895		
	▨	6
84.528		
	▨	16
79.162		
	▒	20
73.796		
	░	25
68.430		—
Sites included		95

Mean: 83.672 Ω/□
Median: 79.649 Ω/□
Standard deviation: 12.163 Ω/□

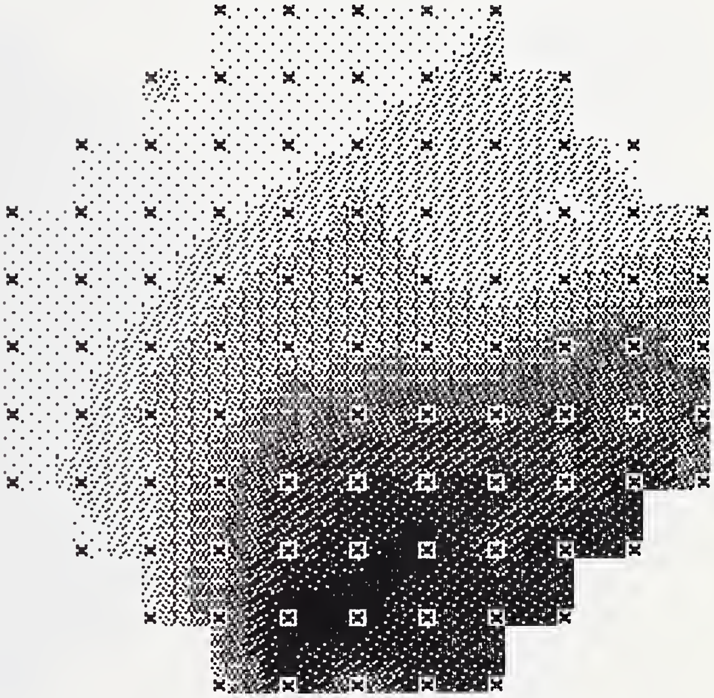


Figure D-17. Wafer map of n^+ sheet resistance, Device no. 9.

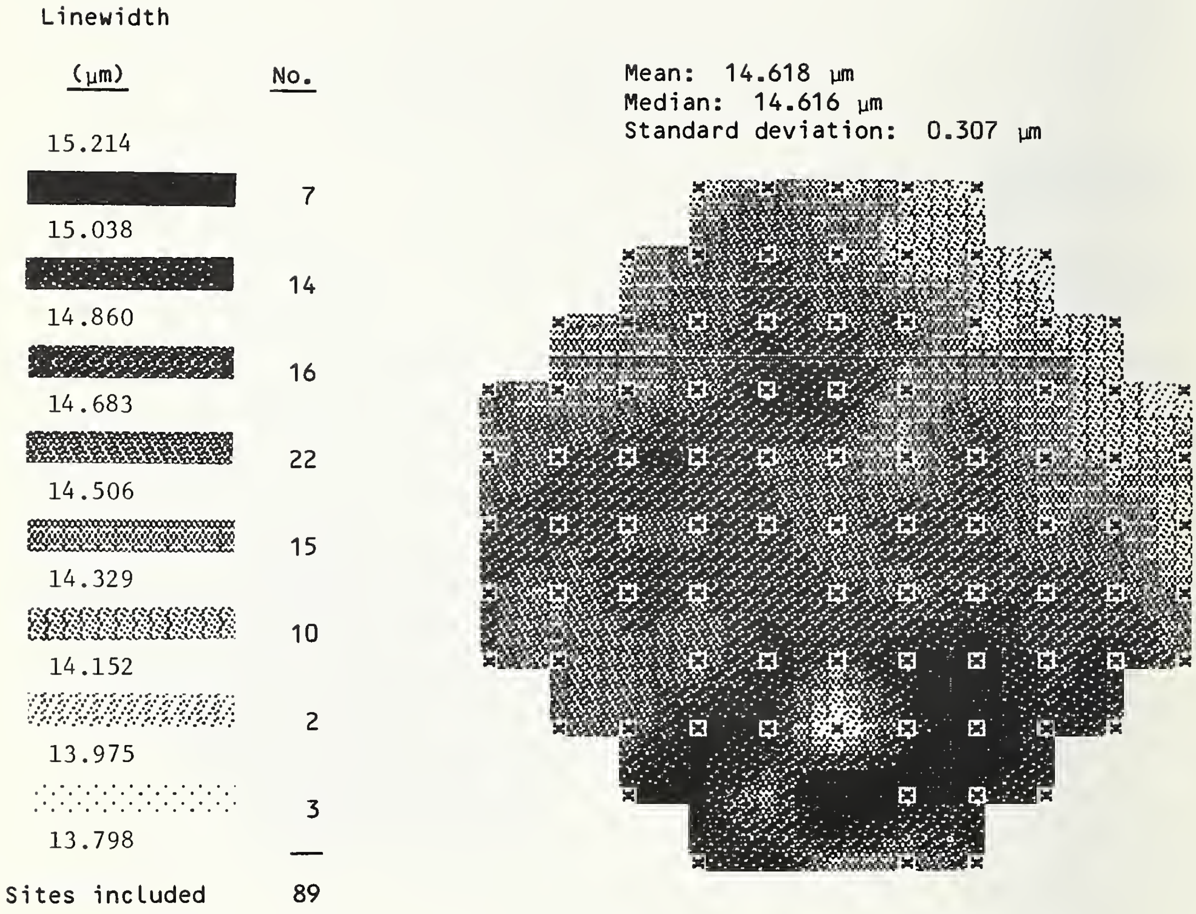


Figure D-18. Wafer map of n^+ cross-bridge sheet resistor linewidth, Device no. 9.

Resistance (Ω/□)	No.
104.117	
■	5
101.739	
▓	11
99.362	
▓	11
96.984	
▓	9
94.606	
▒	4
92.228	
▒	15
89.851	
░	23
87.473	
⋯	14
85.095	
Sites included	92

Mean: 92.949 Ω/□
Median: 90.896 Ω/□
Standard deviation: 5.405 Ω/□

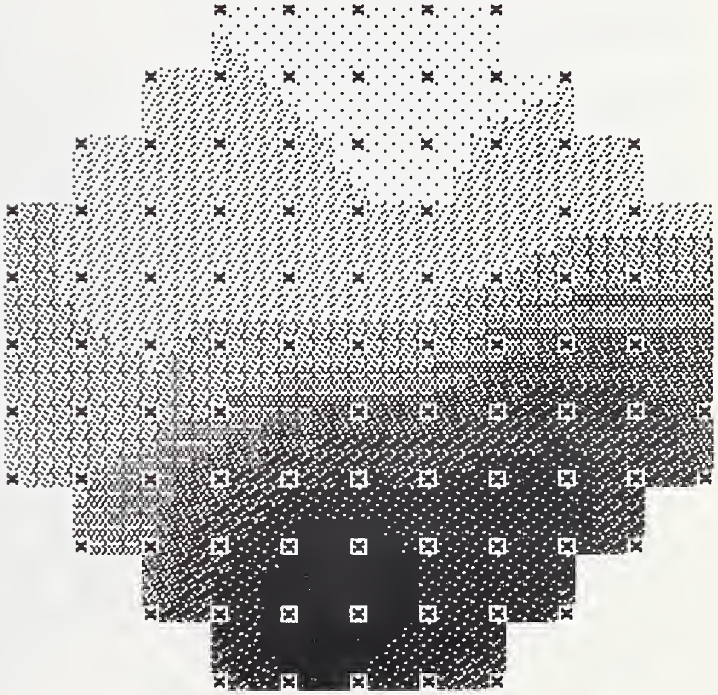


Figure D-19. Wafer map of p^+ sheet resistance, Device no. 10.

Linewidth (µm)	No.
15.931	
■	2
15.682	
▩	6
15.423	
▩	14
15.184	
▩	25
14.934	
▨	21
14.685	
▨	14
14.436	
▒	5
14.186	
░	3
13.937	
Sites included	90

Mean: 14.932 µm
Median: 14.932 µm
Standard deviation: 0.381 µm

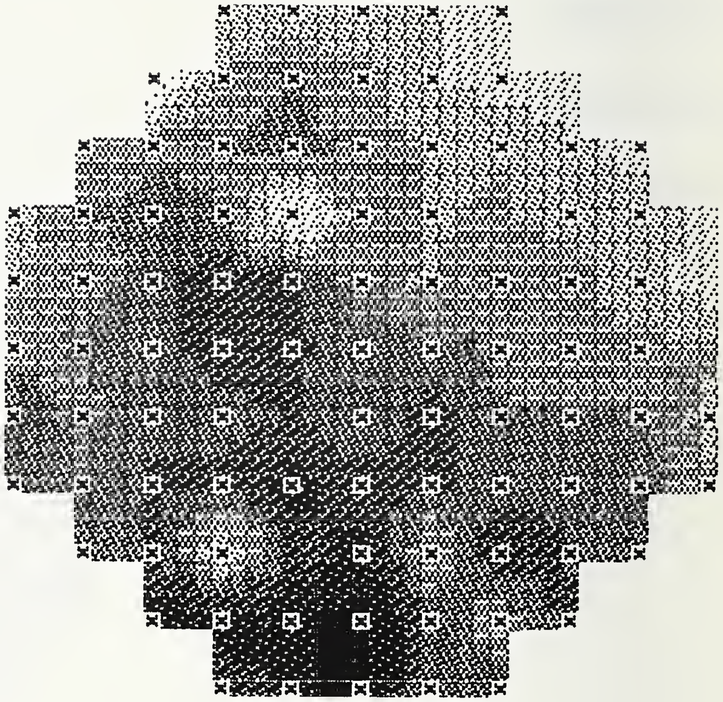


Figure D-20. Wafer map of p^+ cross-bridge sheet resistor linewidth, Device no. 10.

Resistance (Ω/□)	No.
126.150	
■	10
122.007	
▩	15
117.864	
▩	11
113.721	
▩	12
109.578	
▨	6
105.435	
▨	9
101.292	
▧	16
97.150	
░	12
93.007	
Sites included	91

Mean: 109.50 Ω/□
Median: 109.80 Ω/□
Standard deviation: 9.793 Ω/□

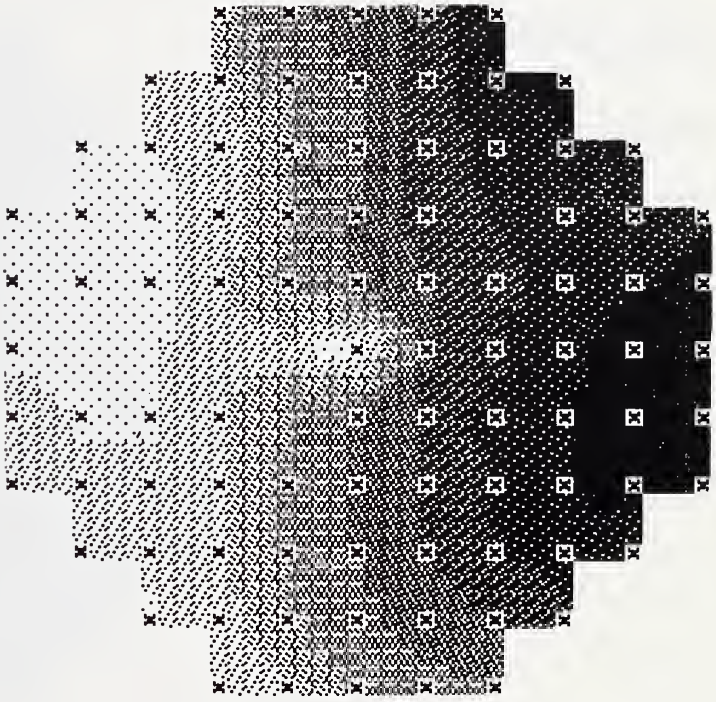


Figure D-21. Wafer map of p^+ doped poly sheet resistance, Device no. 11.

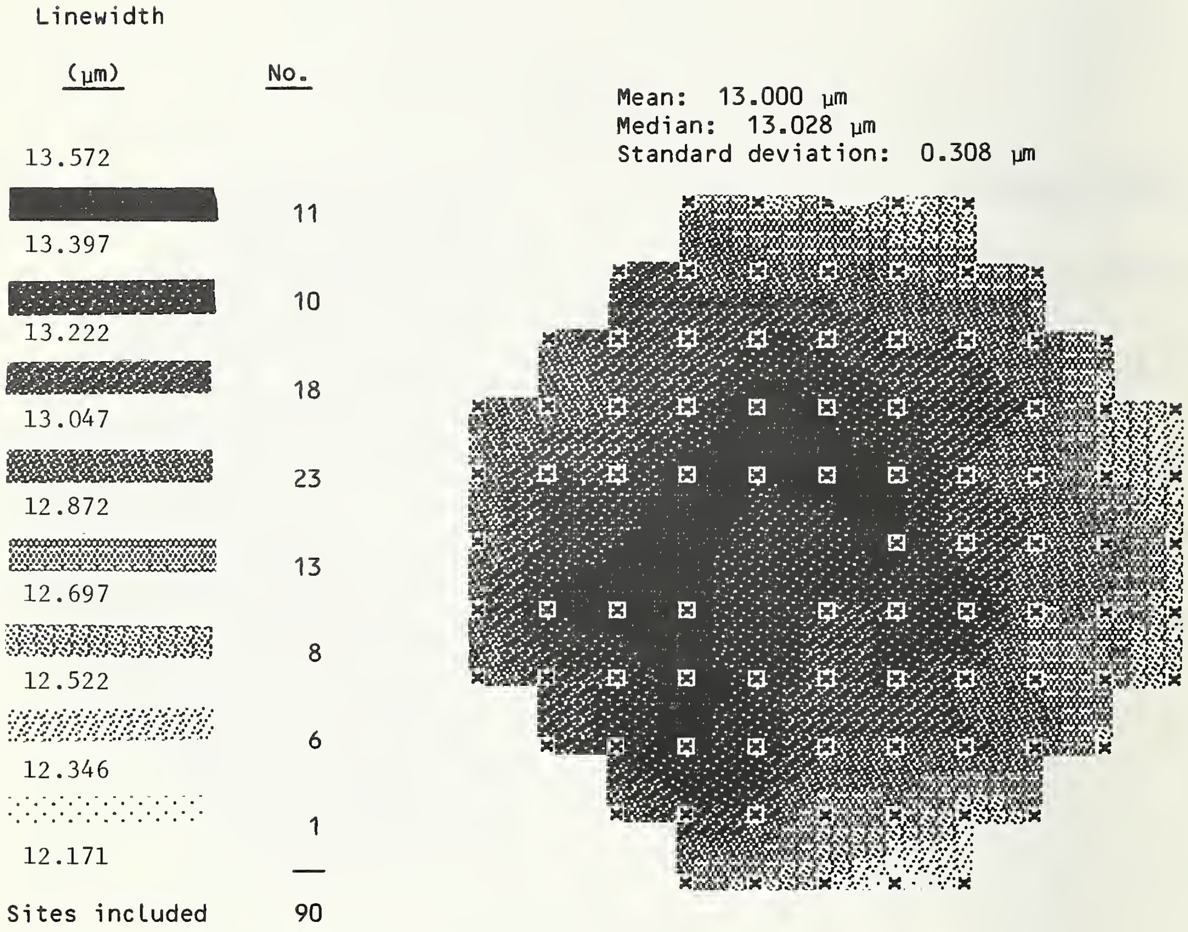


Figure D-22. Wafer map of p^+ doped poly cross-bridge sheet resistor linewidth, Device no. 11.

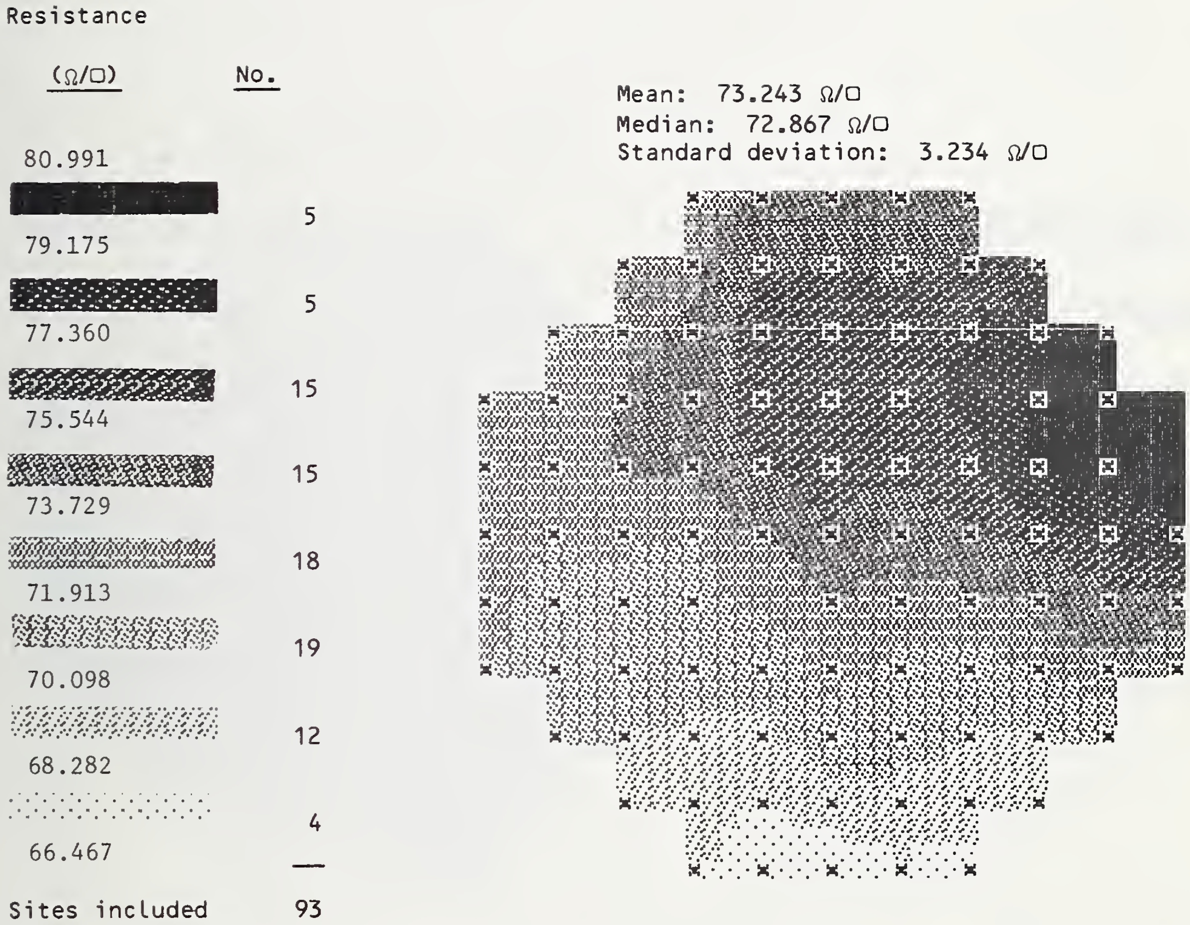


Figure D-23. Wafer map of n^+ doped poly sheet resistance, Device no. 12.

Linewidth (µm)	No.
13.536	
█	12
13.390	
▓	13
13.244	
▓	14
13.099	
▓	14
12.953	
▒	16
12.807	
▒	10
12.662	
░	6
12.516	
⁚	5
12.370	—
Sites included	90

Mean: 13.028 µm
Median: 13.048 µm
Standard deviation: 0.293 µm

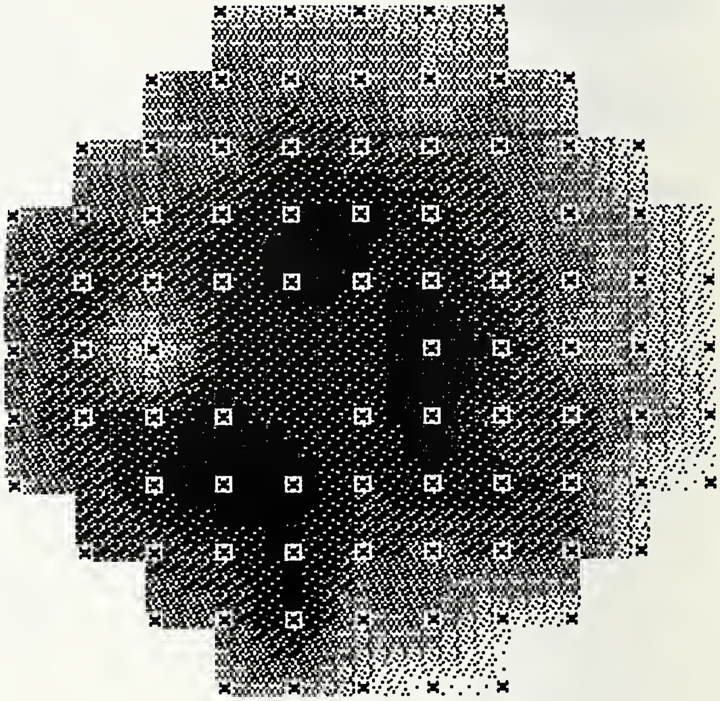


Figure D-24. Wafer map of n^+ doped poly cross-bridge sheet resistor linewidth, Device no. 12.

Resistance (Ω)	No.
7490.8	
■	6
6783.3	
▓	8
6083.8	
▓	18
5380.2	
▒	19
4676.7	
▒	12
3973.2	
░	8
3269.7	
░	14
2566.2	
⋯	10
1862.5	
Sites included	95

Mean: 4927.2 Ω
Median: 4936.7 Ω
Standard deviation: 1458.9 Ω

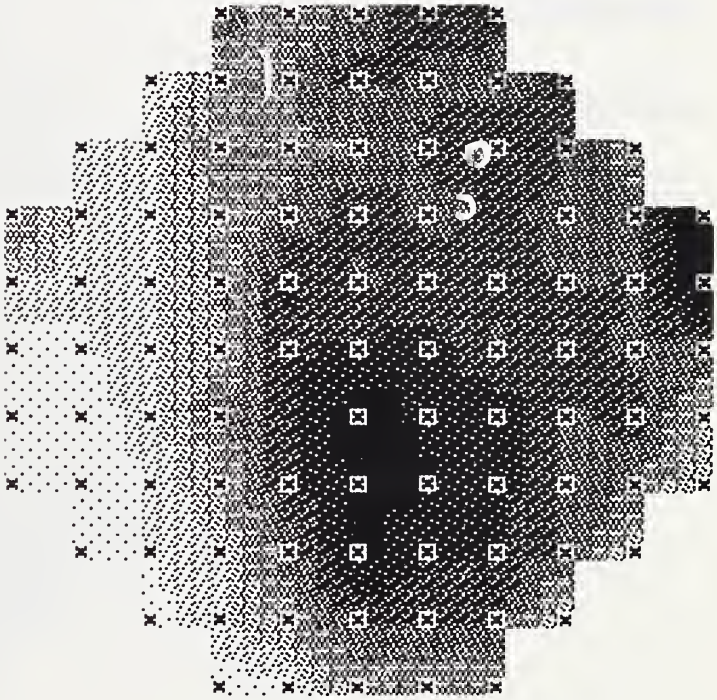


Figure D-25. Wafer map of metal-to-p^- contact resistance, Device no. 16.

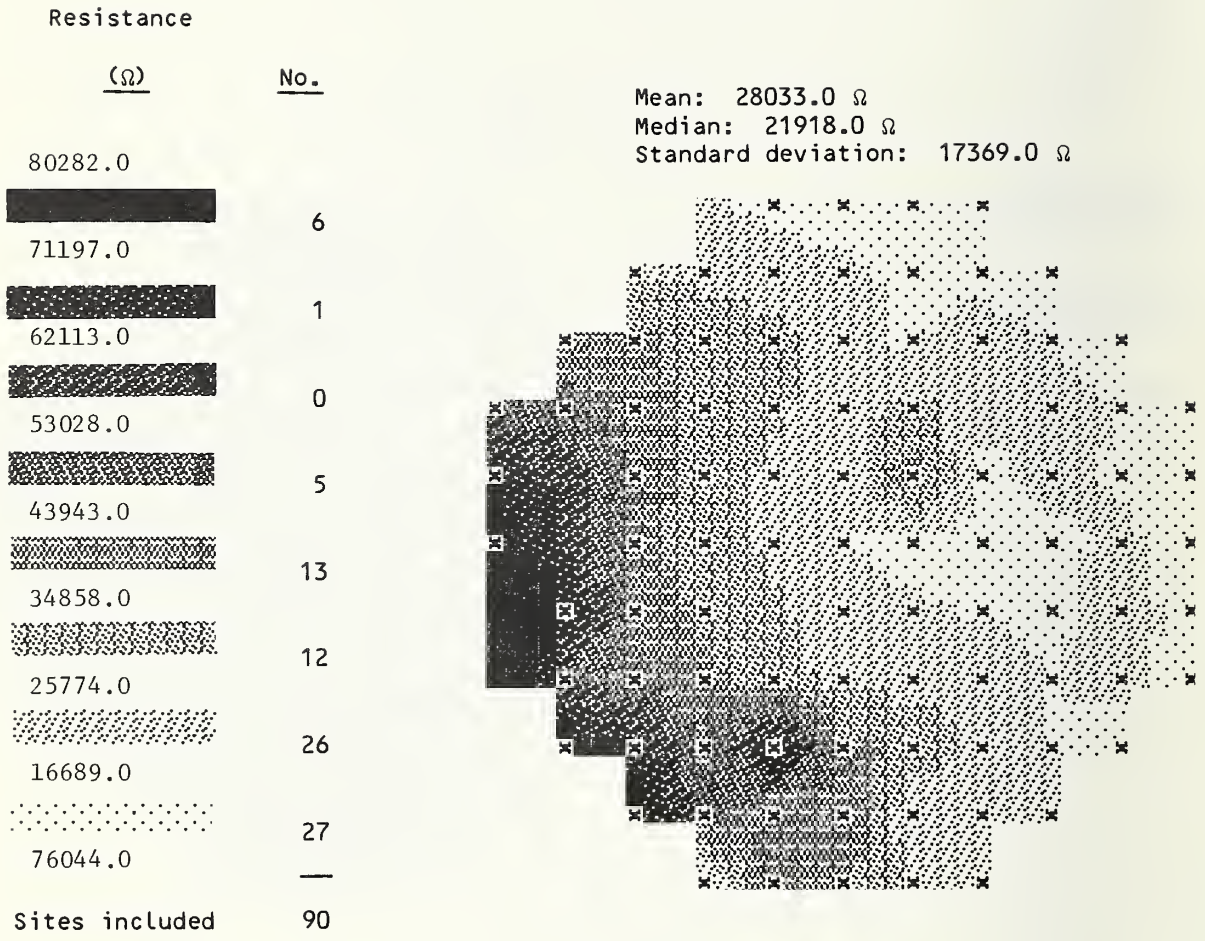


Figure D-26. Wafer map of metal-to-n^- contact resistance, Device no. 17.

Resistance (Ω)	No.
7.390	
█	3
6.851	
▓	1
6.312	
▓	15
5.774	
▒	17
5.235	
▒	5
4.696	
░	16
4.157	
░	20
3.619	
⋯	14
3.080	
Sites included	91

Mean: 4.752 Ω
Median: 4.350 Ω
Standard deviation: 1.077 Ω

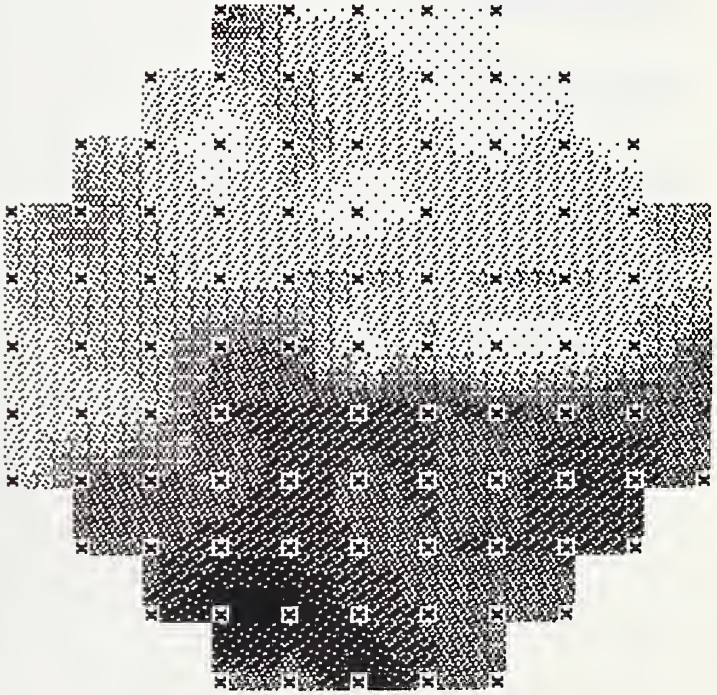


Figure D-27. Wafer map of metal-to-p^+ contact resistance, Device no. 18.

Resistance (Ω)	No.
290.720	
■	5
255.004	
▩	3
219.288	
▨	2
183.571	
▦	2
147.855	
▓	6
112.139	
▒	7
76.422	
░	7
40.706	
⁘	59
4.990	
Sites included	91

Mean: 63.423 Ω
Median: 19.860 Ω
Standard deviation: 76.862 Ω

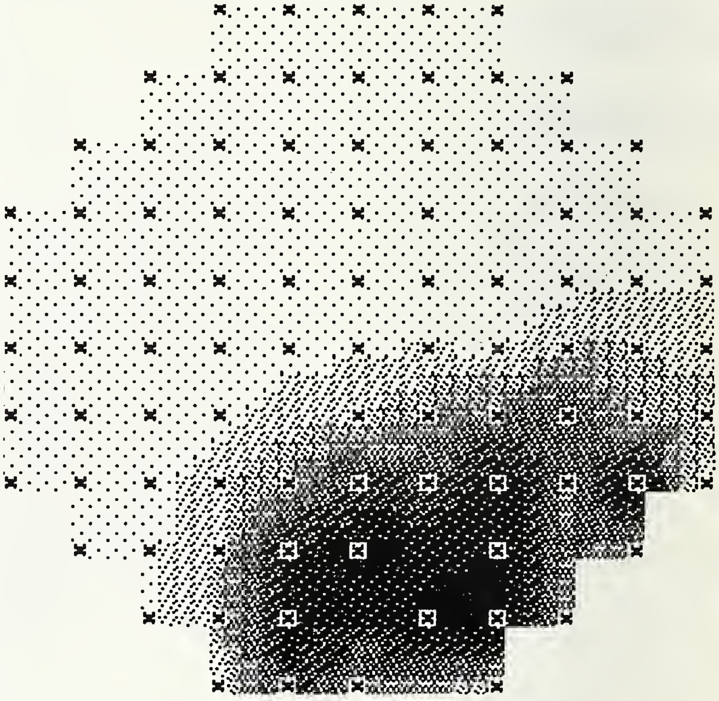


Figure D-28. Wafer map of metal-to-n^+ contact resistance, Device no. 19.

Resistance (Ω)		No.
5.976		
	■	2
5.661		
	▩	2
5.347		
	▩	10
5.033		
	▓	18
4.719		
	▨	12
4.405		
	▒	16
4.090		
	░	18
3.776		
	⋯	13
3.462		
Sites included		91

Mean: 4.415 Ω
Median: 4.388 Ω
Standard deviation: 0.570 Ω

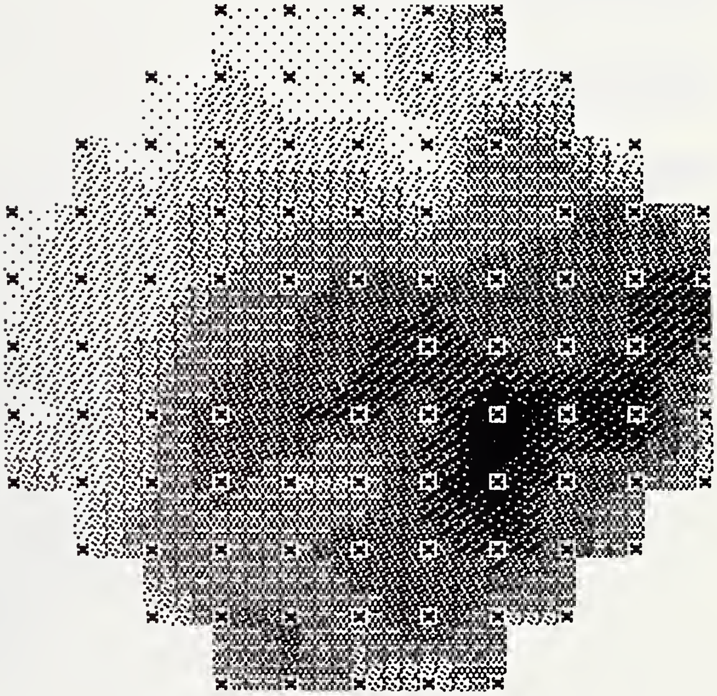


Figure D-29. Wafer map of metal-to-p^+ doped poly contact resistance, Device no. 20.

Resistance (Ω)	No.
4.878	
█	2
4.607	
▓	4
4.335	
▓	7
4.064	
▒	13
3.793	
▒	17
3.522	
▒	15
3.250	
░	22
2.979	
░	11
2.708	—
Sites included	91

Mean: 3.524 Ω
Median: 3.498 Ω
Standard deviation: 0.493 Ω

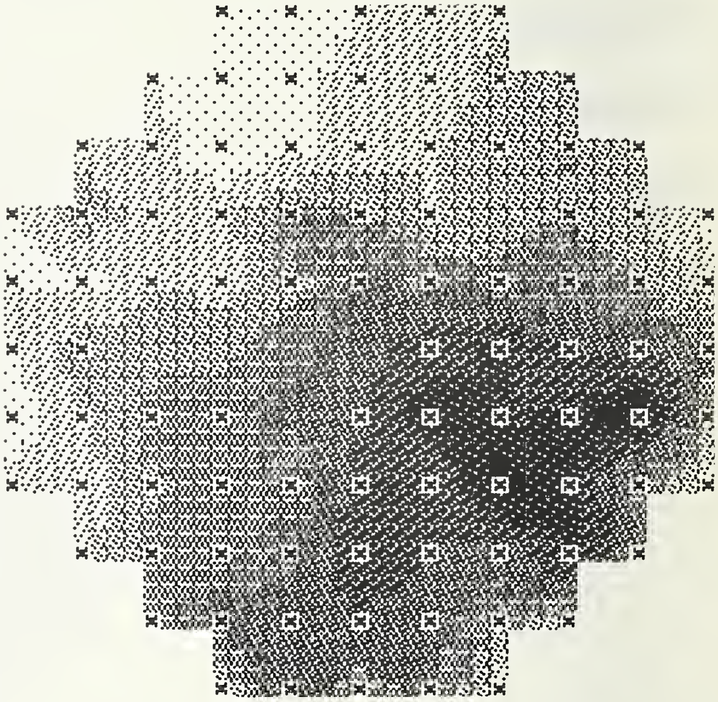


Figure D-30. Wafer map of metal-to-n^+ doped poly contact resistance, Device no. 21.

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☐ Document describes a computer program; SF-185, FIPS Software Summary, is attached.

11. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here)*

A Process Validation Wafer (PVW) is a wafer containing only test patterns. One PVW accompanies a product lot during the fabrication process. Test patterns NBS-16 and NBS-26 are designed to be used on PVWs. They contain both process parameter test structures and random fault test structures. Eighteen NBS-16 PVWs were fabricated in a radiation-hardened silicon-gate CMOS/SOS process. These PVWs were tested on a high-speed computer-controlled dc test system. Test results from the process parameter test structures were used to establish the baseline electrical parameters for each product lot and to produce an eight-level gray scale wafer map for these parameters. Based on correlations of selected wafer maps, it was possible to identify specific yield-related process problems otherwise unknown to the manufacturer or user.

Test results from two random fault test structures were used to establish a statistically significant data base for identifying and evaluating major yield-limiting fault mechanisms in the process. Test results from a developmental random access fault structure and a gate dielectric integrity array are presented. The results are analyzed for selected PVWs and a major yield-limiting fault mechanism detected. A description of the test pattern and test results, including a drawing of each test structure, recommended test procedure, and design rules, are found in the appendices.

12. KEY WORDS *(Six to twelve entries; alphabetical order; capitalize only proper names; and separate key words by semicolons)*

integrated circuits; microelectronics; process validation wafer; random faults; silicon-on-sapphire; test pattern; test structure; yield.

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